A PHYSICAL MOSFET MODEL APPLICABLE TO EXTREMELY SCALED CMOS IC DESIGN

By

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Abstract of Dissertation Presented to the Graduate School of the University of Florida in Partial Fulfillment of the Requirements for the Degree of Doctor of Philosophy

A PHYSICAL MOSFET MODEL APPLICABLE TO EXTREMELY SCALED CMOS IC DESIGN

By

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Major Department: Electrical and Computer Engineering

A process-based model (UFET) for deep-submicron bulk-silicon MOSFETs is developed and verified with numerical device simulations and measured data. The charge-based model is physical with accountings for the predominant short-channel (e.g., charge sharing, drain-induced threshold reduction and velocity saturation) and extremely scaled-technology (i.e., energy quantization and polysilicon-gate depletion) effects in MOSFETs. The key to UFET is the characterization of the bias-dependent two-dimensional regions near the source/drain junctions which can extend over a significant fraction of the metallurgical channel length. When these two-dimensional regions near the junctions are modeled, the physical charge-sheet model can be applied to the remaining "quasi-two-dimensional" channel length to define the channel current and terminal charges, without resorting to empiricism to account for the short-channel effects. Special attention paid to continuity in the derivation of the model formalism yields a physical C_∞ model applicable to analog and digital CMOS circuit design. The small number of physical, process-based parameters simplifies the model calibration, and renders the model suitable for predictive device/circuit simulation, statistical simulations and circuit sensitivity analyses based on known or presumed process variations.

CHAPTER 1
INTRODUCTION

Bulk-silicon CMOS technology continues to be predominant in VLSI applications due largely to the prohibitive capital equipment costs required for any large shift in processing materials or procedure. Although it has been challenged by GaAs with its higher carrier mobility and silicon-on-insulator (SOI) with its reduced junction capacitances for more than a decade, it has defied predictions that these new technologies would soon dominate; the reality is that these two new technologies remain confined to niche markets at this time.

With this in mind it is important to develop accurate compact models for extremely scaled bulk CMOS devices for use in process development/integration and statistical modeling as well as circuit design. Technology CAD (TCAD) requires integrated, physics-based, CPU-efficient device models for predictive circuit simulation. Although many useful MOSFET models are available, they generally lack an adequate physical basis and/or acceptable computational efficiency, in addition to containing discontinuities in their formulations. With a conventional MOSFET model such as BSIM [Che96], a large number of empirical device model parameters are optimized based on measured data (e.g., via least-squares fitting) for circuit simulation. The needed optimization misses correlations between device model and technology parameters which may yield non-unique (erroneous) circuit simulations.

However, the use of application-specific analytic TCAD tools has been suggested as a viable way of attaining the desired computational efficiency [Mar88] while maintaining a strong physical basis. This approach is exploited through the incorporation of application-specified (i.e., a predetermined device structure) analytic, but semi-numerical, device models in the circuit simulator. Unlike conventional optimization-based parameter extraction, the evaluation of the model parameters is based on an analysis of the device structure using criteria consistent with the device physics. Therefore, the parametric correlations are inherently accounted for, and the sensitivities of device and circuit performance to variations in the fabrication process can be reliably and efficiently predicted.

A bipolar junction transistor (BJT) model that meets the criteria required for pragmatic semi-numerical device/circuit simulation was developed previously [Jeo89, Hon94 and Cha97]. The model is based on linked regional analyses of the device structure, and provides a physical alternative to the widely used empirical Gummel-Poon model [Get78]. With its implementation in SPICE2 [Nag75] and incorporation of the parameter evaluator SUMM [Gre90], a viable mixed-mode BJT device/circuit simulator was created.

The deficiencies of existing compact short-channel MOSFET models preclude predictive simulations and use of the models in this pragmatic approach. As MOSFET channel lengths have been scaled into the deep-submicron region, conventional short-channel circuit models have generally been developed via empirical extensions of physical long-channel models. These extensions were based on empirical modifications to simple one-dimensional characterizations of the electric field to account for the short-channel effects, which are controlled by complex two-dimensional field distributions. Most MOSFET models do not explicitly account for the various short-channel effects; for example, BSIM relies heavily on empirical "fitting" expressions that are intended to account for these effects without distinguishing them. Such approaches were taken to preserve the accuracy and efficiency required for simulation of large circuits, but with the loss of predictive capability. In order to achieve predictive simulation, rigorous two-dimensional analyses of the electric field are necessary, but the required computation expense is undesirable for circuit simulation. This dissertation presents a process-based model for deep-submicron MOSFETs (UFET) that relies on approximate two-dimensional analyses, which are computationally efficient, to account for short-channel effects, viz., threshold voltage reduction due to charge sharing [Sze81], drain-induced charge enhancement [Vee88], drain-induced barrier lowering [Tro79] and channel-length modulation [Sze81]. These solutions of two-dimensional analyses are physically linked and are expressed in simple terms that yield physical insight into device behavior as well as a predictive circuit model with utility for TCAD, e.g., for statistical simulations and circuit sensitivity analyses, as well as for design in extremely scaled technologies.

Chapter 2 addresses extremely scaled MOSFET modeling issues, and presents an overview of the previous generation of bulk MOSFET models highlighting the problems associated with regional analyses. A refined iteration scheme for properly modeling LDD devices is also documented.

Chapter 3 presents the new process-based UFET circuit model which includes quasi-two-dimensional analyses that do not have discontinuous regional boundaries. The model applies directly to extremely scaled MOSFETs with retrograde channel and extended source and drain regions, and comprehensively accounts for short-channel effects, field-dependent mobility, impact ionization and device parasitics. Iterative solution techniques are required in the model formalism to predict channel current, impact-ionization current and quasi-static regional charges (to account for transient charging currents) from technology parameters with minimal reliance on empirical modeling.

Chapter 4 overviews the intrinsic model algorithm and the parasitic/ extrinsic portion of UFET. It also details the implementation of the new model (in both MMSPICE and a platform-independent Application Program Interface) and a unique procedure for process-based parameter evaluation which focuses on a limited number of parameters in each key region of operation. This chapter presents verification of the model based on device simulations and measured data from 0.15μm and 0.25μm CMOS technologies.

Chapter 5 presents a simulation exercise in a 0.1μm technology with MEDICI which highlights the ease of parameter evaluation for this model and the power of a process-based model with strong correlation to process variations. Also presented are the results of a sensitivity study using the mentioned 0.15μm technology for the fabrication of a two-stage folded cascode operational amplifier.

Chapter 6 summarizes this work and presents suggestions for model extensions and future research in this area.

CHAPTER 2
SCALED MOSFET MODELING ISSUES

2.1 Introduction

As CMOS technologies are being scaled to sub-0.1μm gate lengths, it is becoming apparent that conventional methods of MOSFET modeling for circuit simulation are inadequate. For example, the need for model continuity [Haj79] in all regions of operation is inferred when designing circuits for low-voltage digital and analog operation, which accompanies extreme scaling. Further, lateral as well as vertical variations in channel doping for controlling (two- and three-dimensional) short-channel effects [Yan91] imply the need for truly physical modeling, which should not rely on global optimization of model parameters. BSIM3 [Che96] is currently the most widely used model for circuit simulation, but its empirical nature, as reflected by the large number of parameters that require copious amounts of data for parameter extraction, portends limits to its utility for extremely scaled technologies. Although an empirical MOSFET model can be used for circuit design in a mature CMOS technology, it is necessary to have a physical model to facilitate the design of new semiconductor processes and the modeling of how the devices behave under normal process variations, as well as to ease, or even enable the parameter-extraction process. Further, such a physical model may be essential even for circuit design in mature extremely scaled technologies.

In this chapter, a physical model for the bulk MOSFET (QBMOS) implemented in MMSPICE-3.0 [Fos94] will first be reviewed. Then results from a technology transfer with AT&T will be discussed in terms of general implications for all MOSFET modeling, including in SOI. A discussion of model refinements leading towards applications in extremely scaled technologies is also presented as a lead-in to Chapter 3.

2.2 QBMOS: A Physical Bulk MOSFET Model

QBMOS [Gre93a] is a significant extension of the previously developed short-channel, charge-based model for thin-film SOI MOSFETs [Vee88]. The noteworthy extensions are accountings for lightly doped drain/source (LDD/LDS) and impact ionization [Cho91] as well as subthreshold current [Gre93b] in the device structure shown in Figure 2.1. The new four-terminal (source, drain, gate and substrate) model is based on the assumptions of uniform channel doping with a constant depletion depth along the channel. The analysis of the carrier-transport mechanisms in the device requires an iterative numerical solution mainly due to the LDD analysis, which must be physically linked to the channel analysis. The resulting semi-numerical model algorithm is implemented in SPICE2 source code creating MMSPICE-3.0, enabling efficient mixed-mode device/circuit simulation since the key model parameters are either structural or physics-based.

QBMOS is based on a regional approach with physical modeling of the channel current in weak (dominant diffusion current) and strong (dominant drift current) inversion. This regional approach simplifies the channel-current modeling in the two regions, but requires a cubic spline to join these analyses across the moderate-inversion region, which has physically boundaries (V_{TW} and V_{TS}) [Tsi82]. In devices where short-channel effects significantly affect the output characteristics

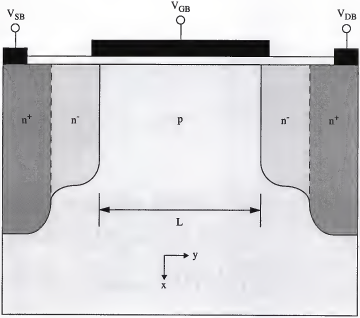

Figure 2.1 Cross-sectional view of a modern bulk MOSFET with LDD and LDS.

of the device, it is necessary to account for the two-dimensional effects on surface potential and inversion charge. The accountings for charge-sharing and drain-induced effects, with the LDD option, are now developed to complete the presentation of the model.

2.2.1 Charge-Sharing

Short-channel devices exhibit two-dimensional effects for $V_{DS} = 0$ due to the lateral electric fields associated with the source and drain junctions. This effect is handled differently in strong and weak inversion.

In strong inversion, a geometrical charge sharing model [Yau74] is used to define an effective gate-controlled body charge (areal) density

$$Q_{b(eff)} = Q_b\left[1 - \frac{x_j}{L}\left(\sqrt{1 + 2\frac{x_{do}}{x_j}} - 1\right)\right], \tag{2.1}$$

where x_j is the source/drain junction depth and x_{do} is the one-dimensional depletion depth. Reducing the effective body charge causes the gate-controlled inversion charge density to increase through Gauss's law (viz., the threshold voltage is reduced) with the accompanying increase in channel current.

The weak-inversion effect of charge sharing is modeled more physically by solving a differential equation resulting from Gauss's law in the regions near the source and drain [Gre93b]:

$$\frac{d^2\Delta\psi_s}{dy^2} \cong \frac{C_{ox} + \frac{\varepsilon_s}{x_{do}}}{\varepsilon_S x_{do}} \Delta\psi_s + \frac{\eta}{2}. \tag{2.2}$$

By modeling the length of these regions, a gradual channel can be defined where the dominant diffusion current can be modeled using one-dimensional theory. A self-consistent assumption for the incremental field at the boundaries of these regions would be $\frac{d\phi_{Fn}}{dy} \gg \Delta E_y$ where ϕ_{Fn} is the electron quasi-Fermi potential, but for simplicity this boundary condition is approximated as $\Delta E_y(L - L_d) \cong 0$. The resulting analysis gives the length of the gradual channel

$$L_e = L - L_s - L_d \tag{2.3}$$

to be used to evaluate the subthreshold channel current with an accounting for charge sharing.

2.2.2 Drain-Induced Effects

In short-channel devices, applied drain biases enhance the channel current through Drain-Induced Barrier Lowering (DIBL) [Tro78] in weak inversion and Drain-Induced Charge Enhancement (DICE) [Vee88] in strong inversion. DIBL results from the direct modulation of the surface potential (ψ_s) by V_{DS}, and DICE is the indirect modulation of the inversion charge implied by the two-dimensional Poisson's equation under the gate.

Application of Poisson's equation in the depletion region can be simplified to Laplace's equation for the incremental change in potential due to V_{DS}:

$$\frac{d^2\Delta\psi}{dx^2} + \frac{d^2\Delta\psi}{dx^2} = 0, \tag{2.4}$$

which can be solved by a quasi-separation of variables:

$$\frac{d^2\Delta\psi}{dx^2} \cong -\frac{d^2\Delta\psi}{dx^2} \cong -\eta, \tag{2.5}$$

where $\eta = \frac{2V_{DS}}{L^2}$ [Vee88]. This first-order extrapolation reduces to the gradual-channel approximation [Sze81] for long-channel devices.

Integrating (2.5) over x yields

$$\Delta E_s(y) = \frac{\Delta\psi_s(y) - \Delta\psi(x_{do}, y)}{x_{do}} - \frac{\eta x_{do}}{2}. \tag{2.6}$$

This expresses the change in the surface transverse electric field as a function of the change in the potentials and the drain bias. Assuming vertical fields in the oxide, Gauss's law is applied at the $Si - SiO_2$ interface with (2.6) to get

$$\Delta Q_c(y) = \left(C_{ox} + \frac{\varepsilon_s}{x_{do}}\right)\Delta\psi_s(y) - \frac{\varepsilon_s \eta x_{do}}{2}. \tag{2.7}$$

In weak inversion, it can be shown that the inversion charge term is much smaller than the terms on the right-hand side of (2.7), so the effect the drain bias is seen as a y-independent increase in the surface potential (DIBL):

$$\Delta\psi_s^{DIBL} \cong \frac{\varepsilon_s \eta x_{do}}{2\left(C_{ox} + \frac{\varepsilon_s}{x_{do}}\right)}. \tag{2.8}$$

The corresponding effect in strong inversion is seen as a y-independent increase in the inversion charge along the entire channel (DICE):

$$\Delta Q_c^{DICE} = -\frac{\varepsilon_s \eta x_{do}}{2}. \tag{2.9}$$

2.2.3 LDD Analysis

The voltage drop across the LDD (V_{LDD}) is computed from the field distribution in the region [Cho91]. Depending on the maximum electric field, there are three possible conditions in the LDD as shown in Figure 2.2. Neutral regions are characterized by constant fields and represent simple ohmic drops. Depletion regions induced in the LDD by the high channel field are characterized by a constant slope assuming the electron charge is negligible,

$$\frac{d|E_y|}{dy} = -\frac{qN_{LDD}}{\varepsilon_s} \equiv -S, \tag{2.10}$$

where N_{LDD} is the doping density in the LDD.

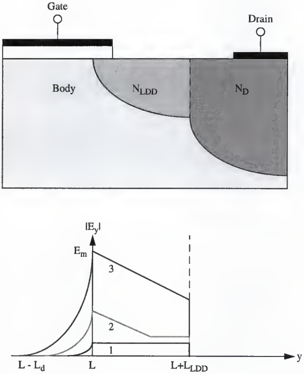

Figure 2.2 Possible lateral electric field distribution in an LDD MOSFET as a function of V_{DS} [Cho91].

The lateral electric field at the body-LDD junction is calculated using the channel-length modulation analyses, but it can easily be shown [Vee88] that it can be accurately approximated as

$$E_m \cong \frac{V_{DS} - V_{LDD} - V_{DS(eff)}}{l_c} \tag{2.11}$$

where $V_{DS(eff)}$ is a result of the channel analysis and l_c is the characteristic length resulting from the analysis of the two-dimensional velocity saturated region.

The calculation of V_{LDD} is done as follows. For $(V_{DS} - V_{LDD}) \leq V_{DS(eff)}$, the maximum electric field is assumed to be small so that only the ohmic drop in the LDD needs to be considered, which corresponds to field distribution '1' in Figure 2.2. Therefore,

$$V_{LDD} = I_{CH}R_{LDD}. \tag{2.12}$$

If $(V_{DS} - V_{LDD}) > V_{DS(eff)}$, all three field distributions '1', '2' and '3' are possible depending on the value of the maximum field. If $E_m \leq \frac{I_{CH}R_{LDD}}{L_{LDD}}$, then case '1' represents the field distribution and (2.12) is used to compute V_{LDD}. If $0 \leq E_m - \frac{I_{CH}R_{LDD}}{L_{LDD}} \leq SL_{LDD}$, condition '2' exists, and the voltage drop across the LDD is calculated using

$$V_{LDD} = \frac{\left(E_m - \frac{I_{CH}R_{LDD}}{L_{LDD}}\right)^2}{2S} + I_{CH}R_{LDD}. \qquad (2.13)$$

For conditions when $E_m - \frac{I_{CH}R_{LDD}}{L_{LDD}} \geq SL_{LDD}$, the entire LDD is depleted and case '3' is applicable with V_{LDD} given as

$$V_{LDD} = L_{LDD}\left(E_m - \frac{SL_{LDD}}{2}\right). \qquad (2.14)$$

An iterative approach is necessitated by the coupling between the channel analysis and the voltage drop across the LDD through the maximum lateral electric field at the body-LDD junction (E_m). In QBMOS, the LDD drop is solved using a secant method with initial iterates of $V^1_{LDD} = 0$ and $V^2_{LDD} = 0.1V_{DS}$.

2.2.4 Impact Ionization

QBMOS accounts for generation current due to (weak) impact ionization involving electrons traversing the high-field region near the drain:

$$I_{Gi} = (M-1)I_{CH} \qquad (2.15)$$

where a local-field model gives the ionization rate as

$$(M-1) = \int \alpha_o e^{-\frac{\beta_o}{|E|}} dy \qquad (2.16)$$

with α_o and β_o being constants.

In the channel, the multiplication factor in (2.16) can be evaluated as [Vee88]

$$(M-1)_{CH} \cong \frac{\alpha_o}{\beta_o}[V_{DS} - V_{DS(eff)}]e^{-\frac{\beta_o l_c}{V_{DS} - V_{DS(eff)}}}. \tag{2.17}$$

The generation current in the LDD is evaluated by numerical integration of the linear field distribution in the depleted LDD region [Cho91]:

$$(M-1)_{LDD} \cong \frac{\alpha_o}{S}\int e^{-\frac{\beta_o}{|E|}}d|E|. \tag{2.18}$$

The sum of (2.17) and (2.18) is the total multiplication factor used to compute I_{Gi} in (2.15).

2.3 Issues Regarding Model Utility

In November 1993, a two-week technology transfer took place between the University of Florida and AT&T (Allentown, Pennsylvania). This consisted of installing MMSPICE-3.0 and applying QBMOS to a 0.9μm CMOS process as well as running a series of thirteen general model tests similar to those presented by Tsividis and Suyama [Tsi94]. These tests are designed to highlight flaws in model physics, modeling approaches and model implementations by qualitatively examining the output characteristics under different DC and AC bias conditions.

The necessity of model continuity generally precludes using regional analyses due to problems introduced by the use of spline functions. This problem with the regional approach is apparent in the QBMOS transconductance plot of

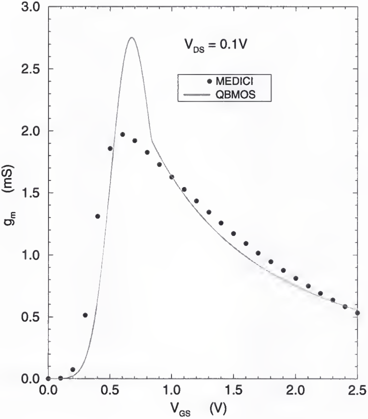

Figure 2.3 Example of cubic spline problem.

Figure 2.3. Since the cubic spline is based on the value of the channel current and the transconductance at the boundaries, the value of the channel current (transconductance) across moderate inversion does not necessarily reflect the physical current (transconductance) but only reflects the function which is necessary to satisfy the boundary conditions. The cubic spline also introduces discontinuities in the higher-order derivatives of the channel current at the boundaries since the cubic spline only guarantees the continuity of the function and its first-derivative. This is apparent in the transconductance plot of Figure 2.4 where the transconductance is continuous but the higher-order derivatives of the channel current are obviously not. A similar discontinuity is also common at the onset of velocity saturation due to the difference in the channel current models above and below saturation. This shows up as a discontinuity in the QBMOS output conductance as shown in Figure 2.5. The use of a regional approach is even further strained when effects (e.g., charge sharing) are not modeled with the same approach in weak and strong inversion. In QBMOS, this introduces a problem for the moderate inversion case since the weak-moderate inversion boundary is not a function of the charge-sharing in the device but the moderate-strong inversion boundary is. In the extreme case, the moderate-inversion region collapses to zero width and the channel current is then discontinuous at this transition as shown in Figure 2.6.

Unlike the moderate-inversion channel current, the moderate-inversion terminal charge modeling in QBMOS is done with a linear interpolation of the terminal charges at the weak- and strong-inversion boundaries. While the integrated charge across moderate inversion is correct with this approach and adequate for

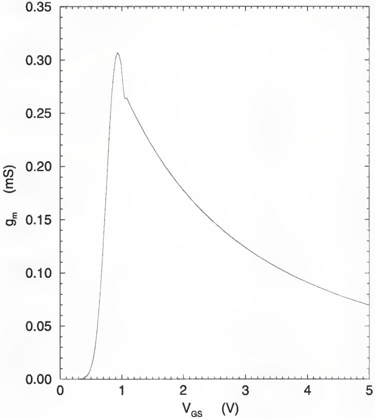

Figure 2.4 Example of transconductance-discontinuity problem.

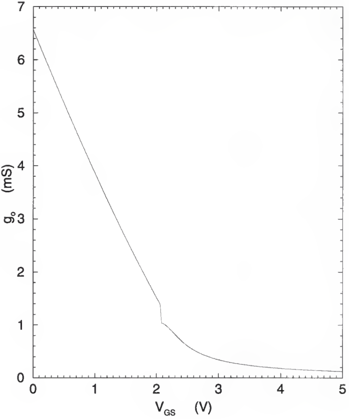

Figure 2.5 Example of output conductance-discontinuity problem.

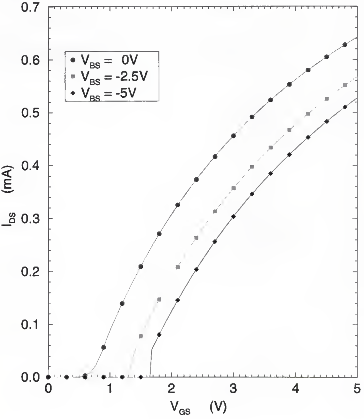

Figure 2.6 Example of charge-sharing problem.

digital simulations, the moderate-inversion capacitance is a constant due to the use of linear interpolation which is problematic for analog applications. The constant capacitance problem is exemplified in Figure 2.7 which shows C_{GG}. Also, note the problem of a constant capacitance in strong inversion for $V_{DS} = 0V$ due to the assumption of a pinned surface potential in strong inversion.

The regional approach has several deficiencies with regard to the continuity of the output characteristics with respect to the terminal voltages. Although discontinuities such as those found in QBMOS are not necessarily a problem for digital simulations, the necessity of continuous derivatives for analog applications does not facilitate the regional approach for use in extremely scaled technologies. The discontinuities also have an adverse effect on the overall convergence and convergence speed of the model. The regional approach can also lead to additional problems when accountings for the same effect differ significantly in strong and weak inversion.

Although the present version of QBMOS is adequate for digital simulation, it is desirable to have a model which is applicable for both digital and analog applications. To accomplish this, QBMOS needs to be improved by removing all discontinuities in the current and terminal charge models to result in a C_{∞} continuity model (i.e., the currents, charges and all derivatives are continuous).

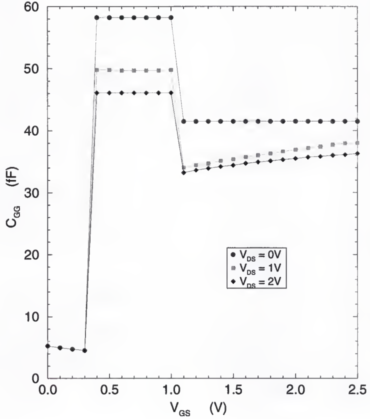

Figure 2.7 Moderate inversion capacitance problem.

2.4 Algorithm Refinements

2.4.1 Improved LDD Loop

A significant time penalty for the intrinsic model arises from the iterative numerical solution required by the presence of a non-ohmic voltage drop across the LDD region. In QBMOS, the LDD drop is iteratively solved using a secant method with initial iterates of $V_{LDD}^{1} = 0$ and $V_{LDD}^{2} = 0.1V_{DS}$ for the bias point solution. Although this method converges to the correct solution, the lack of more precise initial iterates increases the CPU time need to find the solution.

However with (2.11), the analysis can be simplified by substituting this approximation for the maximum electric field into (2.13), yielding

$$V_{LDD} = \frac{\left[\dfrac{V_{DS} - V_{LDD} - V_{DS(eff)}}{l_c} - \dfrac{I_{CH}R_{LDD}}{L_{LDD}}\right]^2}{2S} + I_{CH}R_{LDD}\,. \tag{2.19}$$

Now, (2.19) has V_{LDD} on both sides, and through algebraic manipulation it can be rearranged to

$$\begin{aligned} V_{LDD}^2 - 2\left[V_{DS} - V_{DS(eff)} - \frac{I_{CH}R_{LDD}l_c}{L_{LDD}} - Sl_c^2\right]V_{LDD} \qquad , \\ + \left\{\left[\frac{V_{DS} - V_{DS(eff)}}{l_c} - \frac{I_{CH}R_{LDD}}{L_{LDD}}\right]^2 + 2SI_{CH}R_{LDD}\right\}l_c^2 = 0 \end{aligned} \tag{2.20}$$

which can be easily solved to find the next iterate. This solution method exploits the fact that no quantity in (2.19) is a strong function of V_{LDD}, which is a good approximation across variations in channel length and bias conditions. It is also possible to apply the same approach to (2.14), which results in

$$V_{LDD} = L_{LDD}\left[\frac{V_{DS} - V_{LDD} - V_{DS(eff)}}{l_c} - \frac{SL_{LDD}}{2}\right]. \tag{2.21}$$

Since this equation is linear, it is easy to solve for the next iterate, which is

$$V_{LDD} = \frac{L_{LDD}\left[\frac{V_{DS}-V_{DS(eff)}}{l_c} - \frac{SL_{LDD}}{2}\right]}{1 + \frac{L_{LDD}}{l_c}}. \tag{2.22}$$

Using an initial iterate of $V^1_{LDD} = 0$, the analysis for the channel current is done, resulting in values for I_{CH} and $V_{DS(eff)}$ which lead to a value for V_{LDD} through either (2.12), (2.13) or (2.14) as determined by the depletion condition in the LDD region. If the LDD drop consists of a non-ohmic component, the next iterate for V_{LDD} is then determined using either (2.20) or (2.22), again based on the depletion condition in the LDD. This fixed-point iteration scheme generally converges in two or three iterations, offering a significant improvement over the previously used secant method.

2.4.2 Storage of Initial Iterates

Due to the implicit solutions comprising QBMOS, the terminal characteristics do not have explicit partial derivatives (which are needed to form the Jacobian matrix), and this requires the use of finite difference approximations to define the partial derivatives. This leads to the intrinsic model routine being called four times, once for the bias point and three times for the derivatives with respect to gate, substrate and drain biases. In QBMOS, the intrinsic model calculates the solution of the iterative V_{LDD} analysis using the same initial iterate for each call. However, the bias point solution for the voltage across the LDD can be stored and used as the initial iterate for the subsequent finite difference calls to the intrinsic model routine. The use of the better initial iterate allows the solutions for the perturbed biases to be found in fewer iterations decreasing the cpu time.

The use of this initial iterate, coupled with the implementation of the refined LDD loop, yields a large speed improvement for simulations of devices with significant LDD drops. As shown in Figure 2.8, the original version of QBMOS takes 2.3 times as long to simulate as compared to a version of model that incorporates the previously discussed enhancements. The exemplary simulation was a DC drain characteristic over 6 V_{GS}'s (0.5, 1, 2, 3, 4 and 5V) using 6 different channel lengths (0.5, 0.7, 0.9, 2, 5 and 10 μm). The simulation included a total of 50 V_{DS} bias points for each V_{GS} and channel length for a total of 1800 bias points.

2.5 Summary

MOSFET models based on regional analyses, which rely on a spline functions to join these regions, tend to have problems with function derivatives in the transition regions and also discontinuities of the higher-order derivatives at the boundaries of these regions. These problems imply the need for MOSFET models which are not based on regional analyses and have C_∞ continuity. The continuity

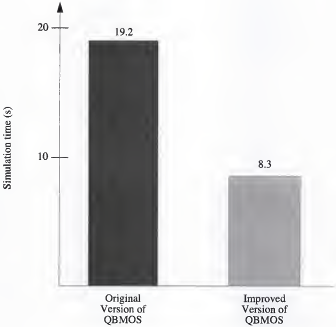

Figure 2.8 Speed enhancement from improved LDD iteration scheme and solution storage technique.

issues should be addressed in the derivation of the model formalism to guarantee that empirical smoothing functions are not used to produce the desired terminal characteristics as done in many MOSFET models. Then the physical integrity of the model, with C_{∞} continuity, can be preserved.

As CMOS technologies are being scaled to sub-0.1μm gate lengths, bulk-silicon devices are moving away from uniformly doped substrates to nonuniform vertical and lateral doping profiles, but many MOSFET models are based on a uniformly doped substrate. MOSFET models for extremely scaled technologies must account for the variations in both the vertical and lateral profiles, and the effects associated with the large vertical fields (i.e., polysilicon-gate depletion and energy quantization) found in these devices while maintaining C_{∞} continuity.

A new MOSFET model is needed which accounts for the physical effects and nonuniform doping profiles found in extremely scaled technologies. The model should be developed avoiding regional analyses due to the inherent continuity problems associated with this approach as shown in this chapter. It should also incorporate the improvements made to QBMOS, i.e., the improved LDD iteration. The resulting model must reliably simulate deep-submicron devices, and enable predictive circuit simulation as noted in Chapter 1.

CHAPTER 3
UFET: A PROCESS-BASED MOSFET MODEL WITH PHYSICAL ACCOUNTINGS FOR SHORT-CHANNEL EFFECTS

3.1 Introduction

Almost twenty years ago, the charge-sheet model was developed [Bre78] for (long-channel) MOSFETs as a physical but more compact alternative to the model of Pao and Sah [Pao66], which requires numerical solutions of integral equations. The charge-sheet model, applicable in all regions of operation, is based on the gradual-channel approximation [Sze81] and is accurate for long-channel devices where short-channel effects are negligible and the saturation of the drain current with increasing drain voltage can be modeled with the pinch-off approximation. However for advanced scaled devices, short-channel effects cannot be ignored, velocity saturation is important and the lengths of the two-dimensional regions near the source/drain junctions can be a significant fraction of the metallurgical channel length. These effects cannot be unequivocally accounted for in the classical charge-sheet formalism, and hence it is not used much today. However, if the two-dimensional regions near the junctions are modeled well, the physical charge-sheet model can be applied to the remaining channel length to define the channel current without having to resort to empiricism to account for the short-channel effects. The development of a new scaled MOSFET model (UFET) based on this concept with accountings for the effects of threshold voltage reduction due to charge sharing

[Sze81], drain-induced conductivity enhancement [Vee88], drain-induced barrier lowering [Tro79], carrier-velocity saturation and channel-length modulation [Sze81] is described in this chapter.

Figure 3.1 shows the typical structure of the deep-submicron enhancement mode (n-channel) bulk-silicon MOSFET, with lightly doped drain (LDD) and source (LDS) regions and retrograded channel doping. Such a regional structure is designed to control most short-channel effects. The original purpose of the LDD was to improve device reliability by reducing peak electric fields in technologies designed to work with large supply voltages. However in advanced devices designed for use with reduced power supplies, these regions are more appropriately referred to as shallow source/drain extensions, having doping concentrations significantly higher than those that yield significant reductions in peak fields, and are used mainly for added control of short-channel effects. The presence of the p^+ region in the retrograded structure reduces the short-channel effects [Yan91] as well by limiting the depletion depth. The new model for this device is simplified by representing the retrograde by a low-high junction, and then characterizing the intrinsic and extrinsic regions separately, incorporating the LDD analysis by a fixed-point iterative solution technique as discussed in Chapter 2.

In the new UFET model, the channel current in the intrinsic device is characterized based on modeling both drift and diffusion for all bias conditions, which eliminates the need for the moderate-inversion spline function and enhances the continuity of the model. The channel current is characterized by integrating the drift and diffusion components over a region in the channel where the two-

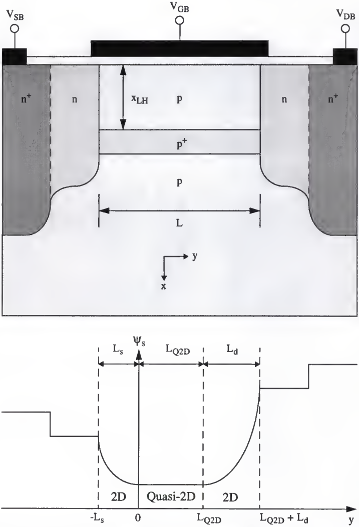

Figure 3.1 The retrograde n-channel MOSFET structure with LDD/LDS regions and a surface potential plot showing the two-dimensional effects of the source and drain junction fields in weak inversion.

dimensional effects are not large, but are merely "quasi-two-dimensional." The first step in calculating the channel current is to characterize the relationship between the applied biases and the surface potential and inversion charge, including short-channel effects based on two-dimensional analysis through the use of Poisson's equation. Characterization of the effective quasi-two-dimensional channel length, based on two-dimensional analyses near the source and drain junctions for arbitrary bias, is part of the model algorithm. The corresponding terminal quasi-static charge modeling, yielding C_{∞} continuity, is then developed using the DC channel-current solution.

3.2 Short-Channel Effects

In scaled devices, the effects of source/drain charge sharing and drain-induced effects (i.e., DIBL and DICE) must be accounted for in the model formalism. More than twenty years ago, Yau [Yau74] introduced a simple model for the threshold voltage of short-channel MOSFETs based on a geometrical partition of the depletion charge among the gate ($Q_{B(eff)}$), source and drain. As the channel length is shortened, the charge shared by the source/drain becomes more significant, with the effective gate-controlled depletion charge and hence the threshold voltage being reduced. Physically, the threshold voltage dependence on channel length is governed by the two-dimensional Poisson's equation in the body,

$$\frac{d^2\psi(x, y)}{dx^2} + \frac{d^2\psi(x, y)}{dy^2} = -\frac{\rho}{\varepsilon_s}, \tag{3.1}$$

which characterizes how the (lateral) source/drain junction fields affect the potential, inversion charge, and even the field in the oxide [Vis85]. Accounting for charge sharing in compact MOSFET models has evolved via improved characterization of threshold voltage for the past two decades. These improvements were initially based on better geometrical charge partitions [Tay78], and more recently on quasi-two-dimensional analyses [Kha93, Liu93]. However, all of the models are limited by the assumption that charge sharing is not a function of the gate bias, and their applicability is limited to characterizing threshold voltage only.

Many models are based on the gradual-channel approximation (GCA), which assumes that $\frac{d^2\psi}{dx^2} \gg \frac{d^2\psi}{dy^2} \approx 0$, implying that there are no significant two-dimensional effects in the channel region of the device. For characterizing the short-channel effects, a new assumption,

$$\frac{d^2\psi}{dx^2} > \frac{d^2\psi}{dy^2} \cong \zeta \neq f(x, y), \tag{3.2}$$

is proposed to be valid over some effective, or quasi-two-dimensional region of length L_{Q2D}; ζ is spatially constant but bias-dependent. As shown in Figure 3.1 (for an n-channel device), the lateral field associated with the source and drain junctions produces regions, with lengths L_s and L_d respectively, in which (3.2) can not be valid. In order to use (3.2), the quasi-two-dimensional channel length must be defined, using two-dimensional analyses to characterize L_s and L_d:

$$L_{Q2D} = L - L_s - L_d \tag{3.3}$$

where L is the metallurgical channel length. Such analyses have been done previously [Gre93b], [ElM77], but not with the generality concerning bias and scalability needed here. The definition of L_{Q2D} and its bias dependence, which are given later, validates (3.2) and allows simpler accounting for the two-dimensional effects in the quasi-two-dimensional channel.

3.2.1 Quasi-Two-Dimensional Potential

Finding a solution to the two-dimensional Poisson's equation in (3.1) is accomplished by assuming that the two-dimensional potential can be written as the linear combination of the one-dimensional solution and a two-dimensional perturbation:

$$\psi(x, y) = \psi_o(x) + \delta\psi(x, y) \tag{3.4}$$

where ψ_o is the one-dimensional solution which is not a function of y and $\delta\psi$ represents the two-dimensional perturbation due to the effects of charge-sharing and/or drain bias. With (3.4), (3.1) is transformed to

$$\frac{d^2(\psi_o + \delta\psi)}{dx^2} + \frac{d^2\delta\psi}{dy^2} = -\frac{\rho_o + \delta\rho}{\varepsilon_s}. \tag{3.5}$$

For *weak inversion* where the inversion charge is negligible, $\delta\rho = 0$, and since the one-dimensional Poisson's equation is

$$\frac{d^2\psi_o}{dx^2} = -\frac{\rho_o}{\varepsilon_s}, \tag{3.6}$$

(3.5) yields a two-dimensional Laplace's equation for the perturbation in the potential:

$$\frac{d^2\delta\psi}{dx^2} + \frac{d^2\delta\psi}{dy^2} = 0. \tag{3.7}$$

For low (but not negligible) longitudinal fields, (3.7) can be solved by quasi-separation of variables:

$$\frac{d^2\delta\psi}{dx^2} = -\frac{d^2\delta\psi}{dy^2} = -\zeta, \tag{3.8}$$

which is consistent with (3.2); ζ models the quasi-two-dimensional effects on ψ. Integrating (3.8) twice in y over the quasi-two-dimensional channel length results in a parabolic potential perturbation $\delta\psi(y)$, which yields an expression for ζ:

$$\zeta \cong 2\frac{\delta\psi(L_{Q2D}) - \delta\psi(0)}{L_{Q2D}^2} + 2\frac{\delta E_y(0)}{L_{Q2D}} \tag{3.9}$$

where the first term predominantly represents the drain-induced effects and the second term predominantly represents the charge-sharing effects. Under "high" drain bias where the drain-induced effects tend to dominate the two-dimensional effects, the parabolic potential has a minimum near the source junction, which implies the approximations $[\delta\psi(L_{Q2D}) - \delta\psi(0)] \rightarrow V_{DS}$ and $L_{Q2D} \rightarrow L$ in (3.9). Underlying these approximations are the boundary values, $\delta\psi(-L_s) = \phi_S - \psi_o$ and $\delta\psi(L_{Q2D} + L_d) = \phi_S - \psi_o + V_{DS}$, where ϕ_s is the source potential, i.e., the equilibrium potential barrier of the source/drain junction, $\phi_S \equiv \frac{E_g}{2q} + V_t \ln\left(\frac{N_B}{n_i}\right)$ where N_B is the channel doping density. The potential ψ is referenced to the unbiased neutral low-doped body. Using these two approximations results in

$$\zeta \cong 2\frac{V_{DS}}{L^2} + 2\frac{\delta E_y(0)}{L_{Q2D}}. \tag{3.10}$$

The second term in (3.10), which dominates at "low" drain bias, can not be explicitly defined. In order to estimate it, let $V_{DS} = 0$ and integrate (3.8) twice in y over the metallurgical channel length. The resulting parabolic $\delta\psi(y)$, with the assumption $\delta\psi\left(\frac{L}{2}\right) = 0$, yields

$$\delta E_y(-L_s) \cong 2\frac{\phi_S - \psi_o(x)}{\frac{L}{2}}. \tag{3.11}$$

The parabolic potential assumption defines a linear variation for the field perturbation. Hence

$$\delta E_y(0) \cong \delta E_y(-L_s) - \zeta L_s(1 + \lambda), \tag{3.12}$$

where $\lambda \geq 0$ accounts for the uncertainty introduced by assuming a parabolic potential in the strongly two-dimensional source region. For $V_{DS} = 0$, $\zeta \cong 2\frac{\delta E_y(0)}{L_{Q2D}}$ in (3.12), which gives

$$\frac{\delta E_y(0)}{L_{Q2D}} = \frac{\delta E_y(-L_s)}{L_{Q2D} + 2L_s(1+\lambda)}. \tag{3.13}$$

Due to the symmetry, $L_s = L_d$ and $L_{Q2D} + 2L_s = L$, which transforms (3.13) to

$$\frac{\delta E_y(0)}{L_{Q2D}} = \frac{\delta E_y(-L_s)}{L + 2L_s\lambda}. \tag{3.14}$$

Using (3.14) to model the charge-sharing effects would require an iterative solution since L_s is a strong function of ζ. In order to make the analysis for the two-dimensional effects suitable for compact modeling, the approximation, $L + 2L_s\lambda \cong L(1 + \mathbf{FCS})$, where FCS is a model parameter greater than, but near 0, is introduced to allow a closed-form solution. Then (3.14) with (3.11) becomes

$$\frac{\delta E_y(0)}{L_{Q2D}} = 4\frac{\phi_S - \psi_o(x)}{L^2(1 + \mathbf{FCS})}. \tag{3.15}$$

However, with (3.15) the expression for ζ in (3.10) is a function of x which is inconsistent with the model in (3.2). Therefore $\psi_o(x)$ in (3.15) is replaced by an average value of the (parabolic) potential across the one-dimensional depletion region (of depth x_{do}), which will be defined later. In order to define this value, the potential is integrated over the depletion depth using the depletion approximation, and the mean value theorem is applied:

$$\begin{aligned}\bar{\psi}_o &= \frac{1}{x_{do}}\int_0^{x_{do}} \psi_o(x)dx \\ &= V_{BS} + \frac{\psi_{so} - V_{BS}}{3}.\end{aligned} \qquad (3.16)$$

Using (3.16) in (3.15) now yields an expression for ζ in (3.10) which is spatially constant:

$$\zeta \cong 2\frac{V_{DS}}{L^2} + 8\frac{\phi_S - \bar{\psi}_o}{L^2(1 + \mathbf{FCS})}. \qquad (3.17)$$

In order to extend the model for *strong and moderate inversion*, it is assumed that the conditions in the channel at threshold adequately represent the conditions below the inversion layer in strong inversion due to the screening of the depletion charge from the gate by the inversion layer. This is effected by limiting the one-dimensional surface potential in (3.16) to less than $\phi_b \equiv 2\phi_F \equiv V_t \ln\left(\frac{N_B^2}{n_i^2}\right)$, which represents the onset of inversion. Analogous to a function presented by McAndrew et al. [McA91],

$$\tilde{\psi}_{so} = \phi_b\left(1 - \frac{\ln\left[1 + e^{A\left(1 - \frac{\psi_{so}}{\phi_b}\right)}\right]}{A}\right), \qquad (3.18)$$

where A is a hard-wired parameter that controls the abruptness of the transition, replaces ψ_{so} in (3.16). The use of (3.18) smooths the transition between the physical approximations in weak and strong inversion; such intrinsic smoothing is physical, in contrast to single-function models [Aro94] that extrinsically and empirically yield smooth terminal characteristics.

3.2.2 Quasi-Two-Dimensional Channel Charge Perturbation

Based on the characterization of ζ, the inversion charge in the quasi-two-dimensional channel region is

$$Q_c = Q_{co} + \delta Q_c \tag{3.19}$$

for all bias conditions. The perturbation δQ_c, which corresponds to $\delta\psi$, is expressed by first integrating (3.8) in x over the one-dimensional depletion region (x_{do}) to describe the perturbation in the vertical field below the inversion layer:

$$\delta E_{x_i} = \frac{\delta\psi_s - \delta\psi(x_{do})}{x_{do}} - \frac{\zeta x_{do}}{2}. \tag{3.20}$$

Gauss's law is then applied over $0 \le x \le x_i$, where $x = 0$ lies just above the $Si - SiO_2$ interface and x_i is the inversion layer thickness:

$$\delta Q_c = \varepsilon_s \delta E_{x_i} - \varepsilon_s \delta E_s. \tag{3.21}$$

Assuming vertical fields in the oxide and substituting (3.20) into (3.21) yields an expression for quasi-two-dimensional channel charge perturbation:

$$\delta Q_c = \left(C_{ox}' + \frac{\varepsilon_s}{x_{do}}\right)\delta\psi_s - \frac{\varepsilon_s \zeta x_{do}}{2}, \tag{3.22}$$

where C_{ox}' represents the variation in the polysilicon potential along the channel as defined later.

The two-dimensional effects (ζ) have now been approximated for all bias conditions, and the corresponding perturbations of surface potential and inversion charge were described. However, the total solution depends on the one-dimensional solution (ψ_o, ψ_{so}, Q_{co}). The solution to the one-dimensional Poisson's equation is now presented.

3.3 One-Dimensional Surface Potential and Inversion Charge

In this section, the one-dimensional relationships among the surface potential (ψ_{so}) the inversion charge (Q_{co}) and the intrinsic biases (V_{GS}, V_{BS} and V_{DS}) in the quasi-two-dimensional channel region are derived in order to characterize the channel current.

Near the center of the n-channel MOSFET structure in Figure 3.1, Poisson's equation is applied in one dimension accounting for hole, depletion and electron charge:

$$\frac{d^2\psi_o}{dx^2} = -\frac{qN_B(x)}{\varepsilon_s}\left[e^{-\beta(\psi_o - V_{BS})} - 1 - e^{\beta(\psi_o - \phi_b)} + e^{\beta(V_{BS} - \phi_b)}\right], \tag{3.23}$$

where $N_B(x)$ is the channel doping concentration, $\beta \equiv \frac{1}{V_t}$, $V_t = \frac{kT}{q}$ and $\phi_b \equiv 2\phi_F \equiv V_t \ln\left(\frac{N_B^2}{n_i^2}\right)$. Multiplying both sides of (3.23) by $2\frac{d\psi_o}{dx}$ and integrating over ψ_o results in a relationship between the electric field and potential at the surface $(x = 0)$:

$$E_{so}^2 = Q_r[e^{-\beta(\psi_{so} - V_{BS})} - 1 + \beta(\psi_{so} - V_{BS}) + e^{\beta(\psi_{so} - \phi_b)} - e^{\beta(V_{BS} - \phi_b)}] \qquad (3.24)$$

where $Q_r \equiv \frac{2q\overline{N_B}V_t}{\varepsilon_s}$ and $\overline{N_B}$, discussed later, represent an effective doping concentration based on the vertical doping transform [Aro87] of the retrograde profile; the vertical field deep in the bulk is implicitly assumed to be zero.

The term on the left-hand side of (3.24) is the surface field in the semiconductor, which with the assumption that the field in the oxide is one-dimensional, can be expressed via Gauss's law in terms of ψ_{so} and ψ_{po}, the potential drop across the polysilicon-gate, which will be analyzed later, as

$$E_{so} = \frac{C_{ox}}{\varepsilon_s}(V_{GS} - V_{FB} - \psi_{so} - \psi_{po}) \qquad (3.25)$$

where $C_{ox} \equiv \frac{\varepsilon_{ox}}{t_{ox}}$ is the gate oxide capacitance, $V_{FB} = \Phi_{MS} - \frac{Q_f}{C_{ox}}$ is the flatband voltage, $\Phi_{MS} = -\frac{E_g}{2q} - V_t \ln\left(\frac{N_B}{n_i}\right)$ is the gate-body work-function difference and Q_f

represents the fixed charge (areal) density in the gate oxide. With (3.25), (3.24) can be solved for ψ_{so} in a few iterations using a second-order Newton's method. Note that (3.24) is identical to the classical charge-sheet equation [Bre78].

3.3.1 Nonuniform Vertical Doping Profiles

The vertical-doping transform [Aro87] enables a step junction to be represented with an effective constant doping. Although the analysis was originally developed to approximate a Gaussian profile with an equivalent (bias-dependent) uniform doping concentration, the analysis is also valid for the case of retrograde channel doping profiles. This transform, for an arbitrary vertical doping profile, is based on four conditions:

- $x_{do} > x_{LH}$
- Conservation of depletion charge under the gate
- Constant surface potential ψ_{so}
- Continuous electric field E_x at $x = x_{LH}$

which lead to the bias-dependent effective doping given by

$$\overline{N_B} = N_B \frac{\psi_I}{\psi_{so} - V_{BS}} \left\{ 1 + \frac{N_{BH}}{N_B} \left[\sqrt{1 + \frac{N_B}{N_{BH}} \left(\frac{\psi_{so} - V_{BS}}{\psi_I} - 1 \right)} - 1 \right] \right\}^2 \tag{3.26}$$

where N_B is the surface doping concentration, N_{BH} is the doping concentration in the p^+ layer and $\psi_I = \dfrac{qN_B x_{LH}^2}{2\varepsilon_s}$ is the built-in potential drop across the lightly doped layer.

However, this analysis assumes that the lightly doped layer is always depleted, which is not the case as bias conditions approach flatband. The term $\frac{\psi_{so} - V_{BS}}{\psi_I}$ is therefore replaced in (3.26) with a smoothly varying function

$$\Gamma = 1 + \frac{\ln\left[1 + e^{A\left(\frac{\psi_{so} - V_{BS}}{\psi_I} - 1\right)}\right]}{A}, \tag{3.27}$$

which is approximately $\frac{\psi_{so} - V_{BS}}{\psi_I}$ when the lightly doped region is depleted and approximately 1 when it is not fully depleted. Thus, $\overline{N_B} \rightarrow N_B$ as the bias conditions approach flatband, which is shown in Figure 3.2 for a typical device. The smoothing function guarantees the continuity of the effective doping concentration and hence ψ_{so}.

The analysis of the effective doping also results in an expression for the depletion depth. Starting from the assumption that the surface region is depleted, the (maximum) depletion depth is

$$x_{do}^{max} = x_{LH}\sqrt{1 + \frac{N_B}{N_{BH}}(\Gamma - 1)}. \tag{3.28}$$

However, when the surface region is not fully depleted the depletion depth is given by the depletion approximation:

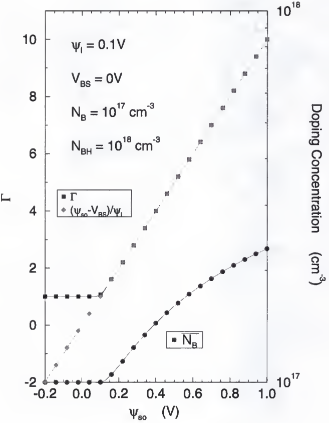

Figure 3.2 The Vertical Doping Transform for a typical device.

$$x_{do} = \sqrt{\frac{2\varepsilon_s \psi_{so}}{qN_B}}. \tag{3.29}$$

Another smoothing function is then used to find the depletion depth under all bias conditions:

$$x_{do} = x_{do}^{max}\left\{1 - \frac{\ln\left[1 + e^{B\left(1 - \frac{x_{do}}{x_{do}^{max}}\right)}\right]}{\ln[1 + e^{B}]}\right\}. \tag{3.30}$$

3.3.2 Nonuniform Lateral Doping Profiles

In scaled devices, it is also necessary to account for nonuniform lateral doping profiles due to halo implants [Tau97] and also the Reverse Short-Channel Effect (RSCE) [Orl87]. A preliminary accounting of these effects is done by using a lateral-doping transform which assumes quasi-Gaussian profiles (with peak doping of N_o and a characteristic length y_o) near the source/drain junctions to modify the surface doping concentration in (3.26) as a function of the channel length [Bru95]:

$$N_B = N_{B(L \to \infty)} + 2\frac{N_o y_o}{L}\left[1 - e^{-\left(\frac{L}{y_o}\right)^2}\right]. \tag{3.31}$$

Thus, the effective N_B is higher than the background doping density, $N_{B(L \to \infty)}$, as illustrated in Figure 3.3

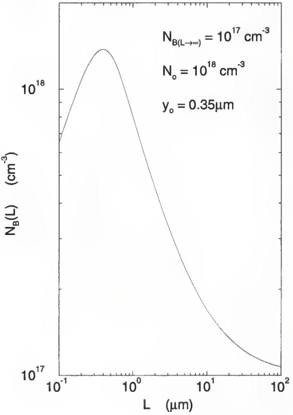

Figure 3.3 The Lateral-Doping Transform for a typical device.

3.3.3 Polysilicon-Gate Depletion

In scaled technologies, the use of dual polysilicon gates is predominant due to the difficulty of designing deep-submicron buried channel PMOS devices [Sha96] and the simplicity of simultaneously implanting the polysilicon-gate and source/drain junctions [Hua93]. However, the implant processing can limit the electrically active doping concentration in the polysilicon [Sch93], which can result in a modification in the device characteristics (both DC and AC) due to the potential drop across the depletion region formed in the polysilicon gate. Although it is possible to achieve good fits to DC data without modeling the polysilicon-gate depletion effect [Aro95], significant errors in the capacitance characteristics will lead to erroneous transient and AC circuit simulations. It is therefore necessary to account for this effect in order to model scaled devices.

Assuming that the two-dimensional effects in the gate oxide and polysilicon are negligible and that the doping profile is uniform near the poly-SiO_2 interface [Hua93], Gauss's law and the depletion approximation give the potential drop across the gate material, based on the electric field in the polysilicon at the interface:

$$E_{po} = \frac{C_{ox}}{\varepsilon_s}(V_{GS} - \Phi_{MS} - \psi_{so} - \psi_{po}) \tag{3.32}$$

and

$$\psi_{po} = \frac{\varepsilon_{poly}}{2qN_{POLY}}E_{po}^2 \tag{3.33}$$

where N_{POLY} is the active doping concentration in the polysilicon gate. Substituting (3.33) into (3.32) results in a quadratic equation for E_{po},

$$\frac{\varepsilon_{poly}}{2qN_{POLY}}E_{po}^2 + \frac{\varepsilon_s}{C_{ox}}E_{po} - (V_{GS} - \Phi_{MS} - \psi_{so}) = 0, \tag{3.34}$$

which can be solved analytically and substituted into (3.33) to find the potential drop across the polysilicon gate.

3.3.4 Quantum Mechanical Effects in the Inversion and Accumulation Layers

In extremely scaled technologies, the high fields at the silicon surface produced by thinner gate oxides and higher channel doping lead to a splitting of the conduction and valence bands into discrete energy sub-bands through quantum mechanical effects. Although this effect can be modeled by assuming an "electrical" t_{ox} larger than the physical gate oxide thickness [Aro95], this introduces the problem of non-physical model parameters and poor capacitance characteristics in the accumulation and moderate inversion regions of operation. The quantization of the carriers in the inversion and accumulation layers can be treated as an effective bandgap widening [Dor94] through a correction to the intrinsic carrier concentration:

$$n_i^{QM} = n_i \exp\left(-\frac{\Delta E_g}{2kT}\right). \tag{3.35}$$

With the assumption of a triangular potential well and the use of a variational method taking into account only the first sub-band, the effective change in the bandgap is

$$\Delta E_g = \frac{13}{9}\kappa\left(\frac{\varepsilon_s}{4kT}E_{so}^2\right)^{1/3}, \tag{3.36}$$

where $\kappa = 4.1\times10^{-10}$ eV-m was extracted from threshold voltage measurements on devices with uniformly doped substrates and 14nm gate oxides. In order to account for increased quantum mechanical effects in thinner oxides where κ may be larger, and also to turn off the quantum mechanical effects in UFET, (3.36) is modified:

$$\Delta E_g = \mathbf{QM}\frac{13}{9}\kappa\left(\frac{\varepsilon_s}{4kT}E_{so}^2\right)^{1/3} \tag{3.37}$$

where **QM** is a model parameter.

Accounting for quantum mechanical effects in the UFET model formalism is done through a modification of Poisson's equation. As proposed by Arora et al. [Aro95], the spatial dependence of the quantum mechanical effect is ignored, and the resulting modification of (3.24),

$$E_{so}^2 = Q_r\left[\frac{n_i^{QM}}{n_i}e^{-\beta(\psi_{so}-V_{BS})} - 1 + \beta(\psi_{so}-V_{BS}) + \frac{n_i^{QM}}{n_i}e^{\beta(\psi_{so}-\phi_b)} - e^{\beta(V_{BS}-\phi_b)}\right], \tag{3.38}$$

can still be solved in a few iterations although the nonlinearity of the equation has increased. Note in (3.38), $\frac{n_i^{QM}}{n_i} \to 1$ and (3.38) reverts to the classical expression for $\Delta E_g \to 0$.

3.3.5 Inversion Charge

After solving (3.38), the magnitude of the one-dimensional inversion charge can be obtained by first integrating Poisson's equation, following the derivation of (3.24), over the predominate inversion layer to define the vertical field below the inversion charge, $E_{x,o}$:

$$E_{so}^2 - E_{x,o}^2 = Q_r\left[\frac{n_i^{QM}}{n_i}e^{\beta(\psi_{so}-\phi_b)} - e^{\beta(V_{BS}-\phi_b)}\right]. \tag{3.39}$$

Then, Gauss's law is used to define the inversion charge:

$$Q_{co}(y) \cong \varepsilon_s\left[\sqrt{E_{so}^2 - Q_r\left[\frac{n_i^{QM}}{n_i}e^{\beta(\psi_{so}-\phi_b)} - e^{\beta(V_{BS}-\phi_b)}\right]} - E_{so}\right]. \tag{3.40}$$

3.4 Quasi-Two-Dimensional Inversion Charge

In order to find the magnitude of the two-dimensional inversion charge in the quasi-two-dimensional channel, Poisson's equation is used in conjunction with Gauss's law, as was done in the derivation of (3.40):

$$\begin{aligned} Q_c(y) &= \varepsilon_s\left[\sqrt{E_s^2 - Q_r\left[\frac{n_i^{QM}}{n_i}e^{\beta(\psi_{so}+\delta\psi_s-\phi_b-V_y)} - e^{\beta(V_{BS}-\phi_b-V_y)}\right]} - E_s\right] \\ &= Q_{co} + \delta Q_c \end{aligned} \tag{3.41}$$

where V_y is the additional quasi-Fermi-level separation at y implied by the drain bias. Although (3.41) is of the same form as (3.40), this is consistent with the charge-sheet approximation where the inversion layer has an infinitesimal thickness and the contribution to Gauss's law due to the two-dimensional effects vanishes:

$$\varepsilon_s \zeta x_i \rightarrow 0 \tag{3.42}$$

where x_i is the inversion layer thickness.

Note that in (3.41) E_s is no longer the one-dimensional surface field, but may be influenced by the two-dimensional effects. The two-dimensional surface field in the semiconductor, with the assumption that the field in the oxide is one-dimensional, can be expressed via Gauss's law in terms of $\psi_{so} + \delta\psi_s$ as

$$E_s = \frac{C_{ox}}{\varepsilon_s}(V_{GS} - V_{FB} - \psi_{so} - \delta\psi_s - \psi_{po}), \tag{3.43}$$

where the use of ψ_{po} assumes that the polysilicon-depletion effects are not perturbed by the two-dimensional effects. It is also assumed that (3.35) and (3.37) adequately represent the quantum-mechanical effects using the one-dimensional surface field.

Using (3.40) and (3.41) it is now possible to define the perturbation in the two-dimensional channel charge as

$$\delta Q_c = Q_c - Q_{co}. \tag{3.44}$$

This result can then be used with (3.22) to fully characterize the two-dimensional effects on potential and inversion charge. The combination of (3.22)

(3.44) must be solved iteratively for $\delta\psi_s$ (~4 iterations worst-case) using a Newton-Raphson algorithm. Note that in weak inversion the two-dimensional effects will result in a $\delta\psi_s \cong \frac{\varepsilon_s \zeta x_{do}}{2\left(C_{ox}' + \frac{\varepsilon_s}{x_{do}}\right)}$ while in strong inversion the resulting effect is a $\delta Q_c \cong -\frac{\varepsilon_s \zeta x_{do}}{2}$. The iterative solution, in terms of the intrinsic biases, guarantees a smooth physical transition between these two effects across the moderate-inversion region.

3.5 Channel Current Model

The current at any position along the channel can be expressed as the sum of the drift and diffusion components:

$$I = W\mu V_t \frac{dQ_c}{dy} - WQ_c v \tag{3.45}$$

where μ is the carrier mobility and v is the electron drift velocity.Using our proposed spatially constant two-dimensional effects assumption in (3.45) enables analytic accounting for all of the two-dimensional effects at any point along the quasi-two-dimensional channel, and hence a solution for the drift/diffusion channel current. In order to find the channel current, (3.45) must be integrated along the channel to find a closed-form solution, which is needed in a compact model to minimize computation time. In order to achieve this goal, the choices for the mobility-(vertical) field model, the velocity saturation model and inversion charge variation model in UFET have been influenced. The need for an explicit channel current equation necessitates the forms of the models to be relatively simple and easily integrated along the channel.

3.5.1 Mobility-Vertical Field Model

The transverse field effect on mobility is dependent on E_x in the channel; it is modeled in terms of the average $\overline{E_x}(y)$ along the channel [Ong87]:

$$\mu_{eff} = \frac{\mu_o}{1 + \Theta_1 \overline{E_x}(y) + \Theta_2 \overline{E_x}^2(y)}, \tag{3.46}$$

where μ_o is the bulk mobility and Θ_1 and Θ_2 are empirical constants. The average transverse field is defined as

$$\overline{E_x}(y) = \frac{C_{ox}}{\varepsilon_s}[V_{GS} - V_{FB} - \psi_s(y) - \psi_p(y)] + \frac{Q_c(y)}{2\varepsilon_s}. \tag{3.47}$$

3.5.2 Velocity-Lateral Field Model

For large drain bias conditions, the high longitudinal electric fields in the channel produce a nonlinear carrier velocity-field relationship. At sufficiently high longitudinal fields, the carrier velocity saturates ($v_{sat} \sim 8\times10^6$ cm/s for electrons). The carrier velocity is modeled by [Aro94]

$$v(y) = \frac{\mu_{eff}\frac{d\psi_s}{dy}}{1 + \Upsilon\frac{\mu_{eff}\frac{d\psi_s}{dy}}{v_{sat}}}, \tag{3.48}$$

where μ_{eff} is the low-(longitudinal)-field mobility and Υ is defined based on an average (longitudinal) electric field as

$$\Upsilon = \frac{\dfrac{\mu \bar{E}_y}{v_{sat}}}{1.5 + \dfrac{\mu \bar{E}_y}{v_{sat}}}. \tag{3.49}$$

3.5.3 Channel Current

With the mobility implied by (3.48), the drift/diffusion current in (3.45) is expressed as

$$I = W \frac{\mu_{eff}}{1 + \Upsilon \dfrac{\mu_{eff} \dfrac{d\psi_s}{dy}}{v_{sat}}} \left(V_t \frac{dQ_c}{dy} - Q_c \frac{d\psi_s}{dy} \right). \tag{3.50}$$

Note that although the mobility implied by (3.48) is only strictly valid for the drift current term, it is used for the diffusion term also. However, since the longitudinal electric field under bias conditions of predominant diffusion current is small, the error introduced is negligible.

Although the inversion charge along the quasi-two-dimensional channel can be defined in terms of the surface potential and quasi-Fermi level separation with (3.41), the variation of the quasi-Fermi level separation along the channel is not known, and the inversion charge must therefore be expressed solely in terms of the surface potential in order to find a closed-form solution for the channel current. For convenience, a reference point, i.e., the virtual source, is defined in the channel (at y = 0), and the potential and inversion charge at all points along the channel are referenced to this point. With the solution for the two-dimensional potential and inversion charge at $y = 0$, $\psi_s(0)$ and $Q_c(0)$ respectively, the change in inversion charge along the channel is defined via Gauss's law as

$$\Delta Q_c(y) \equiv -\varepsilon_s \Delta E_s - \varepsilon_s \Delta Q_b, \tag{3.51}$$

where $\Delta E_s(y) \equiv E_s(y) - E_s(0)$ and $\Delta Q_b(y) \equiv Q_b(y) - Q_b(0)$.

The change in the surface field can be modeled as

$$\Delta E_s(y) = -\frac{C_{ox}}{\varepsilon_s}[\Delta\psi_s(y) + \Delta\psi_p(y)]. \tag{3.52}$$

The earlier analysis for the one-dimensional polysilicon depletion potential results in an expression for the polysilicon depletion potential along the channel,

$$\begin{aligned} \psi_p(y) &= \psi_p(0) + \Delta\psi_p(y) \\ &= \psi_{po} + \Delta\psi_p(y) \\ &= \frac{\varepsilon_{poly}}{2qN_{POLY}}[E_{po} + \Delta E_s(y)]^2 \end{aligned}, \tag{3.53}$$

which can be solved to find $\Delta\psi_p(y)$:

$$\Delta\psi_p(y) = \frac{\varepsilon_s[2E_{po}\Delta E_s(y) + \Delta E_s^2(y)]}{2qN_{POLY}}. \tag{3.54}$$

Substituting (3.54) into (3.52) results in

$$\Delta E_s(y) = -\frac{C_{ox}}{\varepsilon_s}\left[\Delta\psi_s(y) + \frac{\varepsilon_s[2E_{po}\Delta E_s(y) + \Delta E_s^2(y)]}{2qN_{POLY}}\right]. \tag{3.55}$$

In the resulting quadratic equation in ΔE_s only the first-order term is kept in order to allow the resulting channel current equation to be evaluated analytically in the calculation of the drain saturation potential. This is equivalent to assuming a constant depletion capacitance along the channel in the polysilicon gate. The variation in the field is now expressed as

$$\Delta E_s(y) = -\frac{\frac{C_{ox}}{\varepsilon_s}\Delta\psi_s(y)}{1 + \frac{C_{ox}}{\varepsilon_s}x_p} \tag{3.56}$$

where $x_p = \frac{\varepsilon_s E_{po}}{qN_{POLY}}$ accounts for the depletion in the polysilicon-gate.

The variation in the depletion charge along the channel is modeled using the depletion approximation:

$$\Delta Q_b(y) = \sqrt{2q\varepsilon_s\overline{N_B}\psi_{so}} - \sqrt{2q\varepsilon_s\overline{N_B}[\psi_{so} + \Delta\psi_s(y)]}. \tag{3.57}$$

However in order to obtain the desired analytical solution of the drain saturation potential, a Taylor expansion of (3.57) is taken about $\Delta\psi_s(y) = 0$ and the first-order term is kept:

$$\Delta Q_b(y) = \frac{\varepsilon_s}{x_{do}} \Delta\psi_s(y). \tag{3.58}$$

This is equivalent to using a constant depletion capacitance to model the variation in depletion charge. The variation in the inversion charge density along the channel is now expressed as

$$\begin{aligned} \Delta Q_c(y) &= \left(\frac{C_{ox}}{1 + \frac{C_{ox}}{\varepsilon_s} x_p} + \frac{\varepsilon_s}{x_{do}} \right) \Delta\psi_s(y) \\ &= (C_{ox}' + C_d) \Delta\psi_s(y) \end{aligned} \tag{3.59}$$

where C_{ox}' in (3.59) accounts for the variation in the polysilicon potential along the channel.

From the integration of (3.50) over the length (L_{Q2D}) of the quasi-two-dimensional channel, the steady-state channel current is now modeled as

$$I_{CH} = \frac{W}{L_{Q2D}} \overline{\mu_{eff}} \left\{ V_t [Q_c(L_{Q2D}) - Q_c(0)] + \frac{Q_c^2(0) - Q_c^2(L_{Q2D})}{2(C_{ox}' + C_d)} \right\} \tag{3.60}$$

where

$$\overline{\mu_{eff}} = \frac{\dfrac{\mu_{eff}(0)}{1 - B_1 \Delta\psi_s(L_{Q2D}) - B_2 \Delta\psi_s^2(L_{Q2D})}}{1 + \Upsilon \dfrac{\dfrac{\mu_{eff}(0)}{1 - B_1 \Delta\psi_s(L_{Q2D}) - B_2 \Delta\psi_s^2(L_{Q2D})} \Delta\psi_s(L_{Q2D})}{v_{sat} L_{Q2D}}}, \tag{3.61}$$

$$\mu_{eff}(0) = \frac{\mu_o}{1 + \Theta_1\overline{E}_x(0) + \Theta_2\overline{E}_x{}^2(0)}, \tag{3.62}$$

$$B_1 = \frac{[\Theta_1 + 2\Theta_2\overline{E}_x(0)]\dfrac{C_{ox}' - C_d}{2\varepsilon_s}}{(f_B + 1)[1 + \Theta_1\overline{E}_x(0) + \Theta_2\overline{E}_x{}^2(0)]} \tag{3.63}$$

and

$$B_2 = \frac{\Theta_2\left(\dfrac{C_{ox}' - C_d}{2\varepsilon_s}\right)^2}{(2f_B + 1)[1 + \Theta_1\overline{E}_x(0) + \Theta_2\overline{E}_x{}^2(0)]}. \tag{3.64}$$

Note that to obtain (3.63) and (3.64), the approximation $\Delta\psi_s(y) \cong \Delta\psi_s(L_{Q2D})\left(\frac{y}{L_{Q2D}}\right)^{f_B}$ was used to evaluate $\int_0^{L_{Q2D}} \Delta\psi_s dy$ and $\int_0^{L_{Q2D}} \Delta\psi_s^2 dy$; this approximation is not used anywhere else in the model, and in no way implies that a fixed dependence of $\Delta\psi_s(y)$ governs (3.60).

Together (3.40) and (3.59) give the inversion charges at both ends of the channel, which are used in (3.60) to define the channel current. The only unknowns in (3.60) are L_{Q2D} and $\Delta\psi_s(L_{Q2D})$. The next step is then to define the physical locations of the $y = 0$ and $y = L_{Q2D}$ points along the quasi-two-dimensional channel, which leads to an expression for $\Delta\psi_s(L_{Q2D})$ and the primary V_{DS} dependence.

3.6 Two-Dimensional Source-Side Analysis

Focusing on the source region of the MOSFET, Gauss's law is applied to an incremental portion (dy) of the region defined by $-L_s \leq y \leq 0$ and $0 \leq x \leq x_{do}$, where $x = 0$ lies just above the $Si - Si0_2$ interface and x_{do} is the depletion depth at the virtual source, which is used as the fixed lower boundary of the Gaussian surface. Application of Gauss's law results in

$$Q_c(y) + Q_b(0) + Q_f = \varepsilon_s E_x(x_{do}, y) - \varepsilon_{ox} E_{ox}(0, y) - \varepsilon_s \int_0^{x_d} \frac{d^2\psi}{dy^2} dx. \tag{3.65}$$

With the assumption of $\frac{d^2\psi}{dy^2} \neq f(x)$, the vertical field at $x = x_{do}$ can be found by integrating the two-dimensional Poisson's equation,

$$\frac{d^2\psi}{dx^2} = \frac{q\overline{N_B}}{\varepsilon_s} - \frac{d^2\psi_s}{dy^2}, \tag{3.66}$$

twice over the one-dimensional depletion depth and solving for $E_x(x_{do}, y)$:

$$E_x(x_{do}, y) \cong \frac{\psi_s}{x_{do}} - \left(\frac{q\overline{N_B}}{\varepsilon_s} - \frac{d^2\psi_s}{dy^2}\right)\frac{x_{do}}{2}. \tag{3.67}$$

Now using the solution at the virtual source,

$$Q_c(0) + Q_b(0) + Q_f = \varepsilon_s E_x(x_{do}, 0) - \varepsilon_{ox} E_{ox}(0, 0) - \varepsilon_s x_{do} \zeta, \tag{3.68}$$

which provides a convenient reference point, (3.65) can be written, after subtracting (3.68), as

$$\frac{d^2\psi_s}{dy^2} = \frac{2(C_{ox}' + C_d)}{\varepsilon_s x_{do}}[\psi_s - \psi_s(0)] - 2\frac{Q_c(y) - Q_c(0)}{\varepsilon_s x_{do}} + \zeta, \tag{3.69}$$

which is similar to the analysis of current saturation in strong inversion [ElM77]. In that work, the channel was segmented into a region near the source where the gradual-channel approximation can be applied and a high-field region near the drain where the carriers have a saturated drift velocity. Since the current is constant along the channel, the saturated drift velocity implies that the carrier concentration is a constant in this region, and there is therefore no term accounting for any variation in inversion charge $Q_c(y)$, in contrast to (3.69).

However, it should be noted that ζ given by (3.17) is much smaller than $\frac{d^2\psi_{so}}{dx^2}$ for long-channel devices. The ζ implied by (3.2) is

$$\zeta = f\frac{d^2\psi_{so}}{dx^2} \tag{3.70}$$

where $f \ll 1$. This value is used as a minimum value for ζ in the channel-length modulation analyses:

$$\zeta \to \zeta + f\frac{d^2\psi_{so}}{dx^2}. \tag{3.71}$$

The value of f in (3.71) is not critical, and the same results are obtained for a wide range of values $(10^{-2} < f < 10^{-6})$.

In (3.69), the two-dimensional $Q_c(y)$, characterized by (3.41), is not expressed in a manner which allows a closed-form solution to be found. To simplify the model for L_s, an approximate inversion charge distribution which is valid near the source junction is therefore derived. With the assumptions that the drift and diffusion components of the current in (3.45) are in approximate detailed balance in this two-dimensional region and that the low lateral electric field mobility should be used in the two-dimensional source region [Lun96], (3.45) then gives

$$V_t\frac{dQ_c}{dy} \cong Q_c\frac{d\psi_s}{dy}. \tag{3.72}$$

Integrating (3.72) from y = 0 to an arbitrary position then yields the derived approximate inversion charge distribution:

$$Q_c(y) \cong Q_c(0)e^{\frac{\psi_s - \psi_s(0)}{V_t}}. \tag{3.73}$$

Substituting (3.73) into (3.69) now gives

$$\frac{d^2\psi_s}{dy^2} \cong \frac{2(C_{ox}' + C_d)}{\varepsilon_s x_{do}}[\psi_s - \psi_s(0)] - \frac{2Q_c(0)}{\varepsilon_s x_{do}}\left[e^{\frac{\psi_s - \psi_s(0)}{V_t}} - 1\right] + \zeta, \tag{3.74}$$

which must be solved to characterize L_s.

Although (3.74) can be solved numerically via Runge-Kutta or a similar method, the exponential term accounting for the inversion charge makes it impossible to find a closed-form solution. Since the surface potential increases on the order of a few thermal voltages across the two-dimensional region in strong inversion where the characterization of the inversion charge is important, a first-order Taylor expansion of the exponential,

$$2\frac{Q_c(0)}{\varepsilon_s x_{do}}\left[e^{\frac{\psi_s-\psi_s(0)}{V_t}}-1\right]\cong 2\frac{Q_c(0)/V_t}{\varepsilon_s x_{do}}[\psi_s-\psi_s(0)]\,, \tag{3.75}$$

can be used to enable a closed-form solution to be found while adequately accounting for the inversion charge. Although this expansion underestimates the inversion charge in the two-dimensional region as shown in Figure 3.4, the length of this region is controlled mainly by the potential variation that occurs near the quasi-two-dimensional channel, which is well represented by (3.75). The figure also shows that approximately 80% of the length of the two-dimensional region is defined by an increase in surface potential of half a thermal voltage, for which the first-order Taylor expansion is accurate.

With this approximation, the differential equation (3.74) can now be written as

$$\frac{d^2\psi_s}{dy^2}\cong\frac{2\left(C_{ox}'+C_d-\frac{Q_c(0)}{V_t}\right)}{\varepsilon_s x_{do}}[\psi_s-\psi_s(0)]+\zeta\,, \tag{3.76}$$

which can be solved to give the surface potential as a function of position:

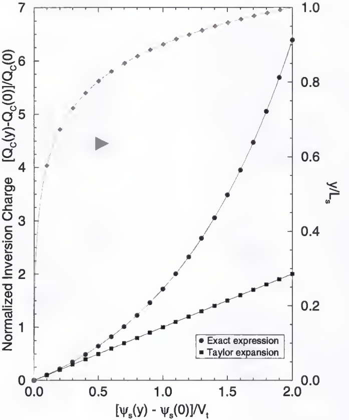

Figure 3.4 The Taylor expansion of the inversion charge underestimates the magnitude of the charge.

$$\psi_s(y) = \psi_s(0) + \left.\frac{d\psi_s}{dy}\right|_{y=0} l_c \sinh\left(\frac{y}{l_c}\right) + \zeta l_c^2\left[\cosh\left(\frac{y}{l_c}\right) - 1\right] \tag{3.77}$$

where $l_c = \sqrt{\dfrac{\varepsilon_s x_{do}}{2[C_{ox}' + C_d - Q_c(0)/V_t]}}$.

The virtual source is located at the potential minimum along the channel, which is equivalent to the $\left.\frac{d\psi_s}{dy}\right|_{y=0} = 0$ condition. Substituting this condition into (3.77) along with the surface potential at the metallurgical junction, $\psi_s(-L_s) \equiv \phi_S$, results in an equation which relates the change in surface potential to the length of the two-dimensional source region:

$$\phi_S = \psi_s(0) + \zeta l_c^2\left[\cosh\left(\frac{-L_s}{l_c}\right) - 1\right]. \tag{3.78}$$

This equation can be solved analytically using the identity which shows that the solution to $A = B\sinh(x) + C\cosh(x)$ is $x = \ln\left(\frac{A + \sqrt{A^2 + B^2 - C^2}}{B + C}\right)$. The result is

$$L_s = l_c \ln\left[\frac{\phi_S - \psi_s(0)}{\zeta l_c^2} + 1 + \sqrt{\left\{\frac{\phi_S - \psi_s(0)}{\zeta l_c^2} + 1\right\}^2 - 1}\right], \tag{3.79}$$

which gives the length of the two-dimensional source region to be separated out from the metallurgical channel length. The length of the two-dimensional source region is a function of all terminal biases (V_{GS}, V_{BS} and V_{DS}) as well as channel length based on the dependencies of $\psi_s(0)$, ζ and $Q_c(0)$.

3.7 Two-Dimensional Drain-Side Analysis

Focusing on the drain region of the MOSFET, Gauss's law is applied to an incremental portion (dy) of the region defined by $L_{Q2D} \le y \le L_{Q2D} + L_d$ and $0 \le x \le x_{do}$, where $x = 0$ lies just above the $Si - SiO_2$ interface and x_{do} is the depletion depth at the virtual source which is used as the fixed lower boundary of the Gaussian surface. Analogous to the previous derivation for L_s, application of Gauss's law using the solution at $y = L_{Q2D}$ as the reference results in

$$\frac{d^2\psi_s}{dy^2} = \frac{2(C_{ox}' + C_d)}{\varepsilon_s x_{do}}[\psi_s - \psi_s(L_{Q2D})] - 2\frac{Q_c(y) - Q_c(L_{Q2D})}{\varepsilon_s x_{do}} + \zeta. \tag{3.80}$$

In the case of saturation, the current analysis in the quasi-two-dimensional channel is coupled to an analysis of L_d that accounts for short-channel effects, as well as to that underlying L_s. In the two-dimensional drain region, the carrier velocity is saturated, and the current in this region can be expressed as

$$I_{CH(sat)} = -WQ_c(y)v_{sat}. \tag{3.81}$$

Since both the (assumed drift) current and the carrier velocity are constant throughout the high-field two-dimensional drain region, the inversion charge density must also be constant; this charge density can be expressed as

$$Q_c(y) = Q_c(L_{Q2D}). \tag{3.82}$$

With the constant inversion charge density assumption, (3.80) can now be expressed as

$$\frac{d^2\psi_s}{dy^2} = \frac{2(C_{ox}' + C_d)}{\varepsilon_s x_{do}}[\psi_s - \psi_s(L_{dd})] + \zeta . \tag{3.83}$$

The derived differential equation (3.83) is similar to the classical derivation of velocity saturated channel -length modulation [ElM77], but with the addition of the ζ term which accounts for short-channel effects.

The solution to (3.83), with the boundary conditions for the potential $\Delta\psi_s(L_{Q2D} + L_d) = V_{DS}$ and lateral field $\left.\frac{d\psi_s}{dy}\right|_{y = L_{Q2D}} = E_{sat} \equiv \frac{v_{sat}}{(1 - \Upsilon)\mu_{eff}(L_{Q2D})}$ implied by (3.48), yields

$$V_{DS} - \Delta\psi_s(L_{Q2D}) = E_{sat} l_c \sinh\left(\frac{L_d}{l_c}\right) + \zeta l_c^2\left[\cosh\left(\frac{L_d}{l_c}\right) - 1\right] \tag{3.84}$$

where $l_c = \sqrt{\frac{\varepsilon_s x_{do}}{2(C_{ox}' + C_d)}}$. Equations (3.3), (3.60), (3.81) and (3.84) provide an implicit solution for L_{Q2D} and $\Delta\psi_s(L_{Q2D})$, and hence $I_{CH(sat)}$.

Although the channel current can be found iteratively, a discontinuity in the derivatives at the onset of velocity saturation would result due to the assumption of a non-physically abrupt onset of velocity saturation. A more physical solution, which leads to a C_∞-continuous model, is found using a system of equations that is asymptotically correct but has a smooth transition between the linear and saturation regions of operation. The first step in finding the approximate solution is to assume that

$$\Delta\tilde{\psi}_s(L_{Q2D}) = \Delta\psi_s^{sat}\left\{1 - \frac{\ln\left[1 + e^{B\left(1 - \frac{V_{DS}}{\Delta\psi_s^{sat}}\right)}\right]}{\ln[1 + e^B]}\right\}; \tag{3.85}$$

B is once again a hard-wired constant that controls the abruptness of the transition from the linear to the saturation region. The perturbed surface potential at the onset of saturation, $\Delta\psi_s^{sat}$, results from equating (3.60) and (3.81) with $L_{Q2D} = L - L_s$ and iteratively solving (which is required by the δ in the velocity-lateral field model) the resulting equation. It is now possible to solve (3.84) with (3.85) for L_d using the identity introduced earlier. The accuracy of this solution is shown in Figure 3.5 which compares $\Delta\tilde{\psi}_s(L_{Q2D})$ to the iterative solution with the discontinuity of the higher-order derivatives for a long-channel device.

If the device is operating in the linear region, the assumptions made for the saturation analysis are invalid, but the resulting equation for the surface potential in the two-dimensional drain region will be of the same form as (3.84):

$$V_{DS} - \Delta\psi_s(L_{Q2D}) = \left.\frac{d\psi_s}{dy}\right|_{y = L_{Q2D}} l_c \sinh\left(\frac{L_d}{l_c}\right) + \zeta l_c^2\left[\cosh\left(\frac{L_d}{l_c}\right) - 1\right], \tag{3.86}$$

where l_c and ζ would now include an accounting for the variation in inversion charge density. It can be shown that the two-dimensional drain region is small in the

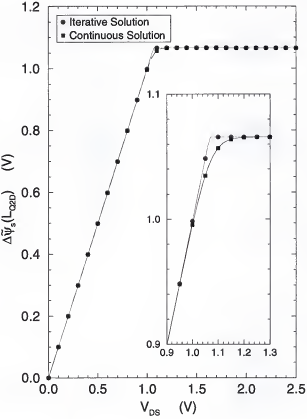

Figure 3.5 Comparison of accuracy for the two solution methods.

linear region of operation since $\Delta\psi_s(L_{Q2D}) \cong V_{DS}$ and $\left.\frac{d\psi_s}{dy}\right|_{y = L_{Q2D}} \gg 0$ for all $V_{DS} > 0$. Equation (3.84) is therefore used for all bias conditions.

3.8 Terminal Charge Modeling

The terminal charging/discharging currents result from the modulation of the space charge as controlled by the time-dependent terminal biases. These currents can be expressed using the quasi-static approximation as

$$\frac{dQ_i}{dt} \cong \sum_j \frac{\partial Q_i}{\partial V_j}\frac{\partial V_j}{\partial t} \tag{3.87}$$

where i=(G,S,D,B) and j=(GS,DS,BS). Note that (3.87) defines nonreciprocal capacitances and transcapacitances that physically reflect the charge dynamics, including short-channel effects, of the four-terminal device.

3.8.1 Quasi-Static Gate Charge

The gate charge is defined by Gauss's law based on a one-dimensional oxide field, integrated over the metallurgical channel length:

$$Q_G = WC_{ox} \int_{-L_s}^{L_{Q2D} + L_d} [V_{GS} - \Phi_{MS} - \psi_s(y) - \psi_p(y)]dy\,, \tag{3.88}$$

which is valid in all regions of operation. This integral can be rewritten as

$$Q_G = W\left\{C_{ox}L[V_{GS} - \Phi_{MS} - \psi_s(0) - \psi_p(0)] - C_{ox}' \int_{-L_s}^{L_{Q2D}+L_d} \Delta\psi_s(y)dy\right\} \tag{3.89}$$

where $\Delta\psi_s(y) \equiv \psi_s(y) - \psi_s(0)$ represents the variation in the surface potential with respect to the solution at the virtual source and C_{ox}' accounts for the variation in the polysilicon depletion potential.

Using the two-dimensional analysis presented in Section 3.6, the integral can be evaluated in the two-dimensional source region resulting in

$$\int_{-L_s}^{0} \Delta\psi_s(y)dy \cong \zeta l_c^2\left[l_c \sinh\left(\frac{L_s}{l_c}\right) - L_s\right] \tag{3.90}$$

where $l_c = \sqrt{\dfrac{\varepsilon_s x_{dD}}{2[C_{ox}' + C_d - Q_c(0)/V_t]}}$.

Similarly, the variation in the potential across the velocity saturated two-dimensional drain region can be evaluated the using the two-dimensional analysis presented in Section 3.7. The resulting integral equation is easily evaluated to give:

$$\begin{aligned}\int_{L_{Q2D}}^{L_{Q2D}+L_d} \Delta\psi_s(y)dy \cong \Delta\tilde{\psi}_s(L_{Q2D})L_d + E_{sat}l_c^2\left[\cosh\left(\frac{L_d}{l_c}\right) - 1\right] \\ + \zeta l_c^2\left[l_c \sinh\left(\frac{L_d}{l_c}\right) - L_d\right]\end{aligned} \tag{3.91}$$

where $l_c = \sqrt{\dfrac{\varepsilon_s x_{dD}}{2(C_{ox}' + C_d)}}$.

The variation in potential in the quasi-two-dimensional channel region is not explicitly found during the calculation of L_{Q2D} and the channel current. However with the use of an average effective mobility, the current can be written at any point along the channel as

$$I_{CH} \cong W \frac{\mu_{eff}}{1 + \delta \frac{\mu_{eff}}{v_{sat}} \frac{d\Delta\psi_s}{dy'}} \{(C_{ox}' + C_d)V_t - [Q_c(0) + (C_{ox}' + C_d)\Delta\psi_s]\} \frac{d\Delta\psi_s}{dy'}, \qquad (3.92)$$

which can be integrated from $y = 0$ to define the potential along the channel:

$$\Delta\psi_s(y) \cong A - \sqrt{A^2 - B\frac{y}{L_{Q2D}}} \qquad (3.93)$$

where $A = V_t - \frac{Q_c(0)}{C_{ox}' + C_d} - \frac{\delta I_{CH}}{W(C_{ox}' + C_d)v_{sat}}$ and $B = \frac{2I_{CH}L_{Q2D}}{W\mu_{eff}(C_{ox}' + C_d)}$. In order to force the condition of $\Delta\psi_s(L_{Q2D}) = A - \sqrt{A^2 - B} = \Delta\tilde{\psi}_s(L_{Q2D})$, B is approximated as $B \cong 2A\Delta\tilde{\psi}_s(L_{Q2D}) - [\Delta\tilde{\psi}_s(L_{Q2D})]^2$, which defines an appropriate value of μ_{eff} in (3.92). However, the resulting equation for the integral of the potential along the channel,

$$\int_0^{L_{Q2D}} \Delta\psi_s(y)dy \cong AL_{Q2D} + \frac{2}{3}\frac{L_{Q2D}}{B}[(A^2 - B)^{3/2} - A^3], \qquad (3.94)$$

has a singularity at $V_{DS} = 0$ where $B \rightarrow 0$. This problem can be eliminated by using a Taylor expansion of (3.94) about $V_{DS} = 0$ and keeping only the first six terms of the series:

$$\begin{aligned} \int_{0}^{L_{Q2D}} \Delta\psi_s(y)dy \cong & \frac{1}{4}\frac{L_{Q2D}}{A}B + \frac{1}{24}\frac{L_{Q2D}a}{A^3}B^2 + \frac{1}{64}\frac{L_{Q2D}}{A^5}B^3a \\ & + \frac{1}{128}\frac{L_{Q2D}}{A^7}B^4 + \frac{7}{1536}\frac{L_{Q2D}}{A^9}B^5 + \frac{3}{1024}\frac{L_{Q2D}}{A^{11}}B^6 . \end{aligned} \tag{3.95}$$

3.8.2 Quasi-Static Channel Charge

The channel charge results from the straightforward integration of the inversion charge density along the metallurgical channel:

$$Q_{CH} = W \int_{-L_s}^{L_{Q2D}+L_d} Q_c(y)dy . \tag{3.96}$$

This integral can be represented similarly to the gate charge with respect to the inversion charge at the virtual source:

$$Q_{CH} = W\left[LQ_c(0) + \int_{-L_s}^{L_{Q2D}+L_d} \Delta Q_c(y)dy\right]. \tag{3.97}$$

Consistent with analysis of the two-dimensional source region, the variation in the inversion charge is approximated using the Taylor expansion of (3.75). The resulting integral is equivalent to (3.90) with an additional constant in front of the integral:

$$\int_{-L_s}^{0} \Delta Q_c(y)dy \cong \frac{Q_c(0)}{V_t} \int_{-L_s}^{0} \Delta\psi_s(y)dy\,. \tag{3.98}$$

Consistent with the assumption of constant channel charge in the two-dimensional drain region, the change in channel charge in this region is simply the change in channel charge at the boundary multiplied by the length of the two-dimensional region:

$$\int_{L_{Q2D}}^{L_{Q2D}+L_d} \Delta Q_c(y)dy \cong (C_{ox}' + C_d)\Delta\tilde{\psi}_s(L_{Q2D})L_d\,. \tag{3.99}$$

Using the variation in inversion charge along the quasi-two-dimensional channel given by (3.59) results in

$$\int_{0}^{L_{Q2D}} \Delta Q_c(y)dy \cong (C_{ox}' + C_d) \int_{0}^{L_{Q2D}} \Delta\psi_s(y)dy\,. \tag{3.100}$$

The result of (3.95) is then used to find the change in channel charge along the effective channel.

3.8.3 Quasi-Static Drain Charge

It is necessary to partition the channel charge between the source and drain. The simple scheme presented by [Oh80] has been chosen to compute the drain charge:

$$Q_D = W \int_{-L_s}^{L_{Q2D}+L_d} \frac{y+L_s}{L} Q_c(y)dy. \tag{3.101}$$

Once again, it is possible to represent the variation in the drain charge along the channel with respect to the inversion charge at the virtual source:

$$Q_D = W\left[\frac{L}{2}Q_c(0) + \int_{-L_s}^{L_{Q2D}+L_d} \frac{y+L_s}{L} \Delta Q_c(y)dy\right]. \tag{3.102}$$

Using the Taylor expansion to represent the inversion charge in the two-dimensional source region results in an expression for the integral in (3.102) across the two-dimensional source region:

$$\int_{-L_s}^{0} \frac{y+L_s}{L} \Delta Q_c(y)dy \cong \frac{Q_c(0)}{V_t} \frac{\zeta l_c^2\left\{l_c^2\left[\cosh\left(\frac{L_s}{l_c}\right)-1\right]-\frac{L_s^2}{2}\right\}}{L} \tag{3.103}$$

where $l_c = \sqrt{\frac{\varepsilon_s x_{dDS}}{2[C_{DX}' + C_d - Q_c(0)/V_t]}}$.

Applying the partitioning scheme to the two-dimensional drain region results in an simple integral which is easily evaluated to give

$$\int_{L_{Q2D}}^{L_{Q2D}+L_d} \frac{y+L_s}{L} \Delta Q_c(y)dy \cong (C_{ox}' + C_d)\Delta\tilde{\psi}_s(L_{Q2D})\frac{L^2-(L-L_d)^2}{2L}. \tag{3.104}$$

Using (3.59) to represent the variation in the inversion charge along the channel, the partitioning scheme results in

$$\int_0^{L_{Q2D}} \frac{y+L_s}{L}\Delta Q_c(y)dy = (C_{Dx}'+C_d)\left[\int_0^{L_{Q2D}} \frac{y}{L}\Delta\psi_s(y)dy + \frac{L_s}{L}\int_0^{L_{Q2D}} \Delta\psi_s(y)dy\right]. \quad (3.105)$$

The second integral on the right-hand side of (3.105) is evaluated in (3.94). With the use of (3.93), the weighted first integral of potential can be approximated as

$$\int_0^{L_{Q2D}} \frac{y}{L}\Delta\psi_s(y)dy \cong \frac{1}{2}AL_{Q2D} + \frac{2}{3}\frac{A^2L_{Q2D}}{B^2}[(A^2-B)^{3/2}] - \frac{2}{5}\frac{L_{Q2D}}{B^2}[(A^2-B)^{5/2}]$$
$$-\frac{4}{15}\frac{L_{Q2D}}{B^2}A^5 \quad . (3.106)$$

As was the case in defining the gate charge, a Taylor series is taken about the singularity at $V_{DS} = 0$ to give:

$$\int_0^{L_{Q2D}} \frac{y}{L}\Delta\psi_s(y)dy \cong \frac{1}{6}\frac{L_{Q2D}}{A}B + \frac{1}{32}\frac{L_{Q2D}}{A^3}B^2 + \frac{1}{80}\frac{L_{Q2D}}{A^5}B^3$$
$$+\frac{5}{768}\frac{L_{Q2D}}{A^7}B^4 + \frac{1}{256}\frac{L_{Q2D}}{A^9}B^5 + \frac{21}{8192}\frac{L_{Q2D}}{A^{11}}B^6. \quad (3.107)$$

With (3.103), (3.104) and (3.107), (3.102) gives Q_D.

3.8.4 Quasi-Static Source and Body Charges

With the use of the charge partitioning model, the source charge is expressed as

$$Q_S = W \int_{-L_s}^{L_{Q2D}+L_d} \left(1 - \frac{y+L_s}{L}\right) Q_c(y)dy\,. \qquad (3.108)$$

However, this integral need not be evaluated since the source charge can be expressed as

$$Q_S = Q_{CH} - Q_D\,. \qquad (3.109)$$

The body charge is computed using the condition of charge neutrality:

$$Q_B = -(Q_G + Q_{CH} + Q_f WL)\,, \qquad (3.110)$$

where Q_f is the fixed charge (areal) density in the oxide.

3.9 Conclusions

A bulk MOSFET model for extremely scaled CMOS which relies on structure-dependent parameters was derived to physically account for one- and two-dimensional effects including charge sharing and drain-induced effects. This is uniquely done by defining a portion of the channel where the two-dimensional effects are approximately constant and by using smoothing functions to define transitions between valid physical approximations. The quasi-two-dimensional channel length, L_{Q2D}, is bias-dependent allowing reliable prediction of current and other device characteristics. UFET is C_∞-continuous and process-based, which makes it an ideal candidate for process integration, statistical/sensitivity studies and circuit simulation in extremely scaled CMOS technologies.

CHAPTER 4
UFET IMPLEMENTATION, PARAMETER EVALUATION AND VERIFICATION

4.1 Introduction

The new UFET model formalism presented in Chapter 3 along with the LDD analysis and local-field impact-ionization model of Chapter 2 has been implemented in both MMSPICE-4.0 and a simulator-independent API (Application Program Interface). After the model implementation is discussed, the intrinsic model parameters introduced in the model formalism and the additional models for the extrinsic circuit elements are presented. Proper evaluation of these model parameters is necessary in order to reliably and efficiently use UFET. A method of obtaining the process-based model parameters, which relies on knowledge of the device physics in all regions of operation and of device structure, is presented and highlights the usefulness of process-based modeling where the model parameters correlate with the actual process. This methodology is demonstrated with a typical retrograde device simulated in MEDICI [Tec92] across channel length and bias. After a comparison to the simulated DC and AC data, UFET is applied to devices in two deep-submicron technologies to assess the model against measured data.

4.2 UFET Implementation

The network representation of UFET is shown in Figure 4.1. The implementation of the model involved developing a subroutine (SSRMOD) to effect

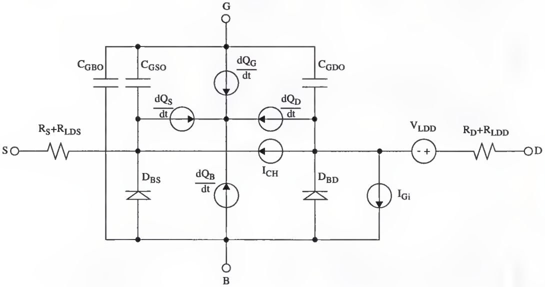

Figure 4.1 Network representation of the four terminal charge-based bulk MOSFET model.

the model formalism as described in Chapter 3. The structure of the intrinsic model routine is shown in Figure 4.2. Since UFET does not use a regional approach, as in [Gre93a], the boundaries for moderate inversion are not needed, and the channel current and terminal charges are calculated using single functions which improves the continuity and convergence properties.

4.2.1 MMSPICE

The new model formalism presented in Chapter 3 (UFET) has been implemented in MMSPICE [Jeo90, Gre93a] version 4.0, an enhanced version of SPICE2 [Nag75] which contains a physical charge-based BJT/HBT model [Hon94] in addition to the standard device models. The model is implemented as a series of subroutines (see Figure 4.3) which calculate the equivalent currents and conductances of a MOSFET. QBFET, which is similar to the subroutine MOSFET in the original SPICE2 code, calls routines that analyze the intrinsic (QBID) and extrinsic (QBEC) regions of a device. QBID in turn calls SSRMOD repeatedly to find the currents (I_{CH} and I_{Gi}), the conductances and transconductances of the currents and the capacitances and transcapacitances associated with the intrinsic-region charges (QG, QB, QS and QD), using a finite-difference method. The extrinsic charge storage is then accounted for in QBEC.

4.2.2 Application Program Interface

In the course of evaluating the UFET model, several deficiencies (e.g., lack of AC modeling and transient simulation problems) of the underlying implementation in MMSPICE became apparent. It was determined that the best of

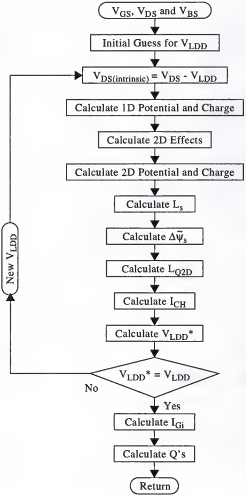
V_{GS}, V_{DS} and V_{BS}
Initial Guess for V_{LDD}
$V_{DS(intrinsic)} = V_{DS} - V_{LDD}$
Calculate 1D Potential and Charge
Calculate 2D Effects
Calculate 2D Potential and Charge
Calculate L_s
Calculate $\Delta\tilde{\psi}_s$
Calculate L_{Q2D}
Calculate I_{CH}
Calculate V_{LDD}*
$V_{LDD}^* = V_{LDD}$
No
Yes
New V_{LDD}
Calculate I_{Gi}
Calculate Q's
Return

Figure 4.2 Flowchart of model algorithm (SSRMOD).

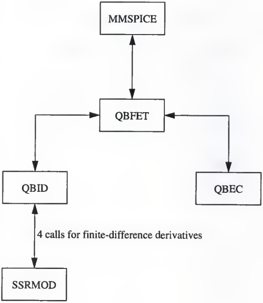

Figure 4.3 MMSPICE-4.0 Implementation.

course of action was to implement UFET in a standard (simulator independent) API which allows different simulator platforms to use identical model source code. Using this Type-I interface [New95], UFET was glued to SPICE3e2 [Qua92].

The Type-I interface is designed to capture the critical elements of a MOSFET model in a single copy of the source code which can be easily distributed and installed on any simulator platform as shown in Figure 4.4. This is accomplished (see Figure 4.5) by defining a set of data structures to hold model and instance data and using a predefined subroutine name for the various calculations necessary in a MOSFET model.

Since the interface is restricted to a four-terminal MOSFET with a predefined matrix stamp, several effects can not be included. For instance, the parasitic source/drain resistances must be bias-independent, and there is no provision made for modeling self-heating or non-quasi static effects. Within these limitations, the interface still provides advantages over the standard method of hard-wiring a model into a simulator. The interface allows the distribution of simulator-independent model code as either source or object code which guarantees that the same model is being used across platforms. This also simplifies the work needed to upgrade the models as research continues.

4.3 Instance and Model Parameters

The model is based on eight instance parameters (see Table 4.1) and 31 model parameters shown in Table 4.2. The instance parameters vary among transistors in a technology or circuit and are the gate length (**L**) and width (**W**), the areas/perimeters of the source (**AS**, **PS**) and drain (**AD**, **PD**), the device temperature

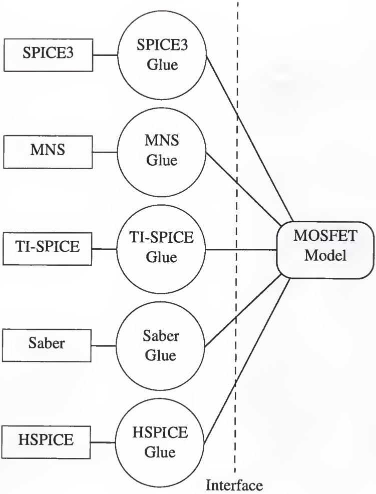

Figure 4.4 Diagram of the Type-I standard interface to MOSFET models.

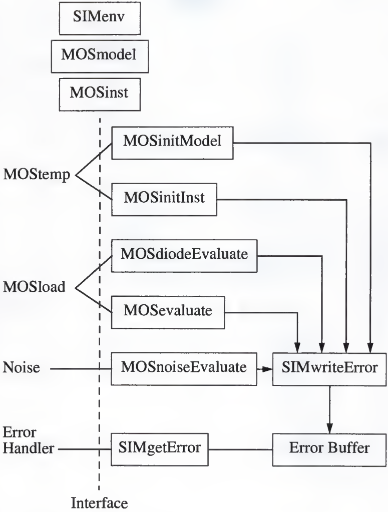

Figure 4.5 Design of the Type-I standard interface to MOSFET models.

Table 4.1 MOSFET Instance Parameters

Name	Description	Units	Default	Typical Value
ND	Drain Node	-	-	-
NG	Gate Node	-	-	-
NS	Source Node	-	-	-
NB	Body Node	-	-	-
MNAME	Model Name	-	-	-
L	Gate length	m	1.0e-6	0.1e-6
W	Gate width	m	1.0e-5	1.0e-5
AD	Drain area	m^2	0	1.0e-11
PD	Drain perimeter	m	0	
AS	Source area	m^2	0	1.0e-11
PS	Source perimeter	m	0	
M	Multiple device option	-	1	1
TEMP	Device temperature	^oC	Circuit Temperature	-
off	DC analysis with device off flag	-	-	-
IC	Device initial conditions	V	-	-

Note: The parameters **PD**, **PS**, **M**, and **TEMP** are not implemented in MMSPICE, but have been implemented in the API.

Table 4.2 MOSFET Model Parameters

Name	Description	Units	Default	Typical Values
DL	Channel-length reduction	m	0.0	0.1e-6
DW	Channel-width reduction		0.0	0.1e-6
NB	Surface channel doping density	cm^{-3}	1.0e17	1.0e17
NBH	High side doping density	cm^{-3}	1.0e18	1.0e18
XLH	Position of high/low junction in retrograde device	m	1.0	0.05e-6
XJ	Source/Drain junction depth	m	0.1e-6	0.1e-6
TOX	Gate oxide thickness	m	5e-9	5e-9
TPG	Type of gate material: +1) opposite to body -1) same as body 0) Aluminum	-	+1	+1
NPOLY	Polysilicon-gate doping density	cm^{-3}	1e25	5e19
NQF	Oxide fixed charge	cm^{-2}	0.0	1.0e-10
WKF	Gate work function difference	V	Calculated	-
LLDD	LDD region length (0 for no LDD)	m	0.0	0.15e-6
NLDD	LDD doping density	cm^{-3}	0.0	1e18
RLDD	Specific LDD parasitic resistance	Ω-m	0.0	500e-6
UO	Zero-field mobility	$cm^2/(Vs)$	Calculated	700 (NMOS) 400 (PMOS)
THETA	Linear mobility degradation coefficient	cm/V	1.0e-6	1.0e-6
THETA2	Quadratic mobility degradation coefficient	cm^2/V^2	1.0e-12	1.0e-12
FB	V_{DS}-averaging factor for mobility degradation	-	1.0	1.0
VSAT	Carrier saturated drift velocity	cm/s	1.0e7	1.0e7

Table 4.2 -- continued

Name	Description	Units	Default	Typical Values
AI	Impact-ionization parameter α_0	cm^{-1}	0.0	2.45e6 (NMOS) 3.7e6 (PMOS)
BI	Impact-ionization parameter β_0	V/cm	0.0	1.92e6 (NMOS) 8.0e6 (PMOS)
QM	Quantum mechanical effects modulation factor	-	1.0	1.0
FCS	Short-channel charge-sharing modulation factor	-	0.0	0.1
NO	Peak doping in RSCE/halo	cm^{-3}	0.0	1e18
YO	Characteristic length of RSCE/halo	m	0.0	0.05e-6
CGDSO	Gate-(source + drain) overlap capacitance	F/m	Calculated	1.0e-10
CGBO	Gate-body overlap capacitance	F	0.0	1.0e-0
RDS	Total specific extrinsic resistance	Ω-m	0.0	600e-6
JS	Parasitic diode saturation current density	A/m^2	0.0	1.0e-9
N	Parasitic diode ideality factor	-	1.0	1.0
CJO	Zero-bias parasitic diode junction capacitance	F/m^2	0.0	1.0e-3
MJ	Parasitic diode junction grading factor	-	0.5	0.5
PJ	Parasitic diode junction potential	V	0.8	0.8

Note on differences between MMSPICE and API implementations: The parameters **CGDSO** and **RDS** have replaced **CGDO**, **CGSO**, **RD** and **RS** respectively. In MMSPICE, the extrinsic overlap capacitance and resistance should be divided between the respective source and drain components. The parameters **LLDD** and **NLDD** have replaced **LLD** and **NLD** as used in MMSPICE. Also, the parameter **ULD** has been replaced by **RLDD** which is the quantity actually measured/ evaluated.

(**TEMP**) and the multiple finger option (**M**). The 31 model parameters are assumed to be constant for devices in a given technology and describe the intrinsic and extrinsic portions of the device. Of the 31 model parameters, 20 are physically significant and can be extracted from the device cross-section or doping profiles of the device.

4.3.1 Intrinsic Model Parameters

The intrinsic portion of the device is described by the 23 parameters which define the structure, (approximate) doping profiles and doping dependent parameters. Of these 23 parameters, only seven can not be estimated from information about the process but must be input by the user. The carrier saturation velocity (**VSAT**) is a material constant with a typical value of $\sim 8\times10^{6}$ cm/s. The impact-ionization model relies on two empirical constants (**AI** and **BI**) in order to calculate the impact-ionization rate in the channel and LDD. The transverse-field dependence of the carrier mobility in the channel is modeled by a linear (**THETA**) and quadratic (**THETA2**) dependence on the vertical field, although a recent paper presented a derivation of these two parameters from basic scattering processes [Rei96]. The carrier mobility is also a function of the potential along the channel, and an approximate integral is used with a fitting parameter (**FB**) to determine the channel current.

4.3.2 Extrinsic Model Parameters

The remaining 8 parameters describe the extrinsic portion of the device. In scaled devices, it is a necessity to accurately model the device extrinsics (including interconnects which are not part of UFET) in order to accurately model transient and AC device behavior.

The parasitic junction diodes each have five model parameters with the junctions assumed to be symmetric. The leakage current through the parasitic source diode is [Ant88]:

$$I_{BS} = \mathbf{AS}\ \mathbf{JS}\left(e^{\frac{\beta V_{BS}}{\mathbf{MJ}}} - 1\right), \tag{4.1}$$

where **JS** is the junction leakage current and **MJ** is the junction grading coefficient. The parasitic junction capacitances are assumed to be predominantly due to the area component. The depletion charge associated with the source junction is [McA93]

$$Q_{BS} = \mathbf{AS}\frac{\mathbf{CJO}}{1 - \mathbf{MJ}}\left(1 - \frac{\tilde{V}_{BS}}{\mathbf{PJ}}\right)^{1 - \mathbf{MJ}}, \tag{4.2}$$

with **CJO** being the zero-bias depletion capacitance associated with the junction, **PJ** is the built-in junction potential and $\tilde{V}_{BS} = R{*}\mathbf{PJ} - \frac{\ln[1 + e^{A(R*\mathbf{PJ} - V_{BS})}]}{A}$ continuously models the voltage dependence. The constants R and A are generally extracted under forward-bias conditions but have been hard-wired to reasonable values.

The overlap capacitors are modeled as simple parallel plate capacitors (**CGDSO** and **CGBO**) and contribute to the charging currents shown in Figure 4.1. In addition to the voltage drops across the LDS/LDD regions of the device, the additional extrinsic resistances, e.g., contact resistance, are accounted for with the model parameter **RDS** (= $R_S + R_D$). In order to improve the computation efficiency of the implementation, the ohmic portions of the LDS/LDD drops (R_{LDS} and R_{LDD}) are added to R_S and R_D respectively as shown in Figure 4.1.

4.3.3 Model Parameter Temperature Dependencies

Since the model parameters are physical, the temperature dependencies of the parameters are implemented using published models [Wor98] in a straightforward manner. An example of this is the model for the intrinsic carrier density

$$n_i = 1.45\times10^{16}\left(\frac{T}{300}\right)^{1.5} e^{q\Delta E_G} \tag{4.3}$$

where $\Delta E_G = \frac{1.115}{2k(300)} - \frac{1.16 - 7.02\times10^{-4}\frac{T^2}{T+1108}}{2kT}$. Using this temperature-dependent value of n_i leads to an implicit temperature-dependent threshold voltage through the definition of $\phi_b \equiv V_t \ln\left(\frac{N_B^2}{n_i^2}\right)$.

4.4 General Approach to Parameter Evaluation

Proper evaluation of the model parameters is necessary in order to reliably and efficiently use UFET. Since most of the parameters are based either on the device structure or the underlying physics, the resulting parameter evaluation methodology is relatively straightforward and does not rely on a standard optimizer. The key to this approach is to recognize that a limited subset of the model parameters controls the DC or AC terminal characteristics in a given region of operation. The majority of the model parameters can be evaluated from the DC measured characteristics.

Table 4.3 Technological MOSFET Parameters Used for Verification

Parameter	Value
TOX	5.5 nm
DL	0.05 μm
XJ	0.2 μm
L	0.35 μm
W	20 μm

To start with, an initial set of parameters is assumed, from processing (technology) or 2-D process simulation, e.g., with SUPREM [Tec89]. Since UFET is physical with several structural parameters, this initial evaluation is straightforward and indeed can give very good estimates for the parameter values. The (assumed) initial values for the parameters however need not be known with a great degree of certainty. Once the initial values are obtained, the calibration methodology can be applied in a systematic manner using a short- and a long-channel device. This methodology is demonstrated with a typical retrograde device simulated in MEDICI [Tec92] across channel length and bias. The retrograde MOSFET used for the comparison is based on a device presented at a recent IEDM [Ven95] with the structural and doping parameters shown in Table 4.3 and the channel profile shown in Figure 4.6.

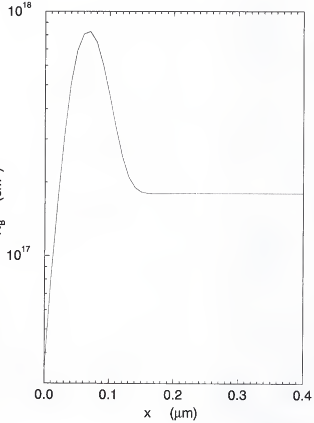

Figure 4.6 Retrograde channel doping profile used in MEDICI.

4.5 Parameter Evaluation for Retrograde Bulk MOSFETs

The model parameters, along with their description are listed in Table 4.2. Also listed are their typical values for current state-of-the-art bulk technologies. Now, given the technology, **TOX** is usually well known, and hence it can be directly specified in the input model card. The critical parameters in the table that usually have to be evaluated are **XLH, NB, NBH, NPOLY, DL, RDS, UO, THETA, THETA2** and **VSAT**. If an LDS/LDD is present in the structure, **LLDD** and **NLDD** must also be estimated. Some of the other parameters (e.g., **FB**) have only a secondary effect on the device characteristics. Hence, parameter evaluation is restricted to only a few structural and physical parameters. The evaluation process will be systematically detailed by considering different regions of operation where these key parameters have characteristic signatures.

4.5.1 Results from Assumed Initial Parameter Values

Based on the channel profile, the initial parameter values can be used to start the parameter evaluation process. The value of **NBH** is assumed to be equal to the peak doping in the channel, and **NB** is set equal to a value between the surface doping concentration and **NBH**. The position of the high-low junction is then estimated to be one-half of the position of the peak doping in the channel. Using the standard mobility curves then provides an estimate of **UO**. The other parameter values are then set to the UFET default values. The parameter values used for this first evaluation are shown in Table 4.4 in the column labeled Level = 0. Predictions of current-voltage characteristics resulting from the use of this initial parameter set are shown in Figures 4.7-4.10. It should be noted that the large error for the short-

Table 4.4 UFET Model Parameters for Evaluation

Parameter	Units	Level = 0	Level = 1	Level = 2	Level = 3	Level = 4	Level = 5
XLH	μm	0.03	0.015	0.015	0.015	0.015	0.015
NB	cm^{-3}	$1x10^{17}$	$1x10^{17}$	$0.4x10^{17}$	$1x10^{17}$	$1x10^{17}$	$1x10^{17}$
NBH	cm^{-3}	$9x10^{17}$	$9x10^{17}$	$9x10^{17}$	$4.7x10^{17}$	$4.7x10^{17}$	$4.7x10^{17}$
UO	$cm^2/(Vs)$	750	750	750	750	900	900
THETA1	cm/V	$1x10^{-6}$	$1x10^{-6}$	$1x10^{-6}$	$1x10^{-6}$	$1.3x10^{-6}$	$1.3x10^{-6}$
THETA2	cm^2/V^2	$1x10^{-12}$	$1x10^{-12}$	$1x10^{-12}$	$1x10^{-12}$	$0.8x10^{-12}$	$0.8x10^{-12}$
RDS	Ω-μm	$400x10^{-6}$	$400x10^{-6}$	$400x10^{-6}$	$400x10^{-6}$	$50x10^{-6}$	$50x10^{-6}$
VSAT	cm/s	$1x10^{7}$	$1x10^{7}$	$1x10^{7}$	$1x10^{7}$	$1x10^{7}$	$1.25x10^{7}$

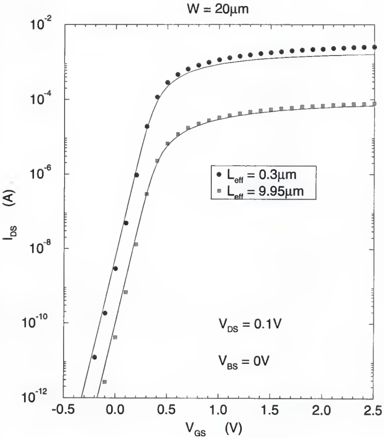

Figure 4.7 Subthreshold plot with $V_{BS} = 0V$ using Level = 0 model parameters.

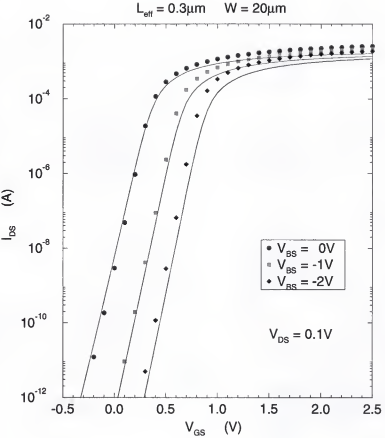

Figure 4.8 Subthreshold plot with $V_{BS} \neq 0V$ using Level = 0 model parameters.

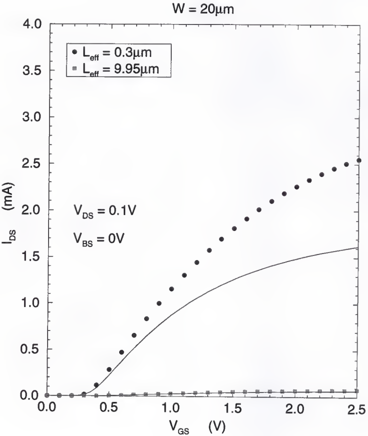

Figure 4.9 Threshold plot with V_{BS} = 0V using Level = 0 model parameters.

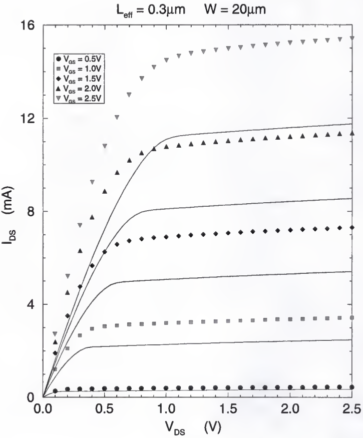

Figure 4.10 Linear-Saturation plot with $V_{BS} = 0V$ using Level = 0 model parameters.

channel device in the threshold plot of Figure 4.9 is due to the default ideal contact in MEDICI. Although a better initial estimate of the parasitic resistances would have been zero in this case, the first stages of the parameter evaluation are done with the UFET default values in order to demonstrate the initial model parameter values need not be very accurate to calibrate the model.

4.5.2 Calibration Based on Subthreshold Characteristics

In the subthreshold region, the current conduction mechanism in a MOSFET is predominantly by carrier diffusion [Sze81], and can hence be modeled in a rather straightforward manner. The current in this region can then be used to obtain information on the position of the high/low junction **XLH**, the (uniform) body doping **NB** and **NBH** (for $V_{BS} \neq 0$), and the lateral source/drain diffusion length **DL**.

Now, **XLH**, **DL**, **NB** and **NBH** are calibrated for a given device at low drain bias. The subthreshold slope is given approximately as

$$S \cong 60\left(1 + \frac{C_d}{C_{ox}}\right) \qquad (4.4)$$

where $C_d \cong \frac{\varepsilon_s}{\mathbf{XLH}}$ is the depletion capacitance and $C_{ox} = \frac{\varepsilon_{ox}}{\mathbf{TOX}}$ is the oxide capacitance. With the initial estimates of the doping concentrations, **DL** and knowledge of **TOX** from the technology, **XLH** can then be tuned to obtain the subthreshold slope. **NB** and **NBH** usually have only a minor effect on subthreshold slope. Using this value of **XLH** gives in the results of Figure 4.11 which use the parameters shown as Level = 1 in Table 4.4.

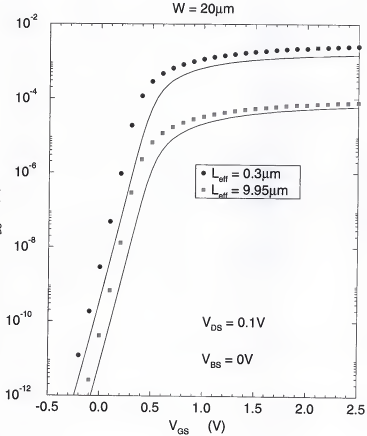

Figure 4.11 Subthreshold plot with V_{BS} = 0V using Level = 1 model parameters.

The current in this region, which depends on the gate-controlled body charge ($Q_B \propto$ **NB*XLH**), can now be used to calibrate **NB**. If necessary, **XLH** may also be fine-tuned to fit both the current and the slope. Note that usually the lateral source/drain diffusion length **DL** is a constant for all channel lengths in a given wafer even when RSCE is significant. To ensure consistency, the calibration procedure may be applied to a range of channel lengths to define an "optimized" **DL** for the given technology based on the current as well as the slope at low and high V_{DS}. The parameters as this stage of the evaluation process are shown in Table 4.4 as Level = 2, and the corresponding plot is shown in Figure 4.12.

If data is available for $V_{BS} \neq 0$, the doping concentration on the high-side of the junction can also be determined from the subthreshold data. The potential drop across the high side of the junction results in a reduction of the body bias effect controlled by the doping concentration. By tuning the doping concentration in this region of the device across several V_{BS}'s, an "optimized" value of **NBH** can be found. If the optimized value of **NBH** is significantly different from the initial estimate, the value of **NB** may also need to be slightly tuned in order to improve the fit at low body bias. This was true in this case due to the large value of **NBH** initially assumed, and this is reflected in the Level = 3 parameters of Table 4.4. The results of the body bias simulations are shown in Figure 4.13

At this stage of the tuning process, **XLH**, **DL**, **NB** and **NBH** are known. The remaining parameters are now extracted in strong inversion.

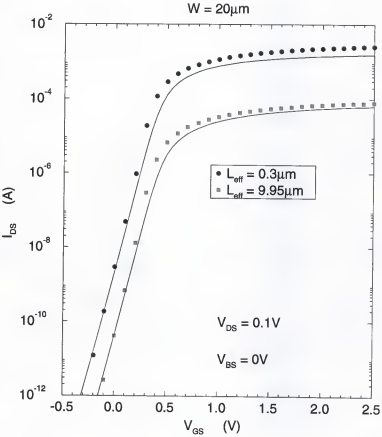

Figure 4.12 Subthreshold plot with V_{BS} = 0V using Level = 2 model parameters.

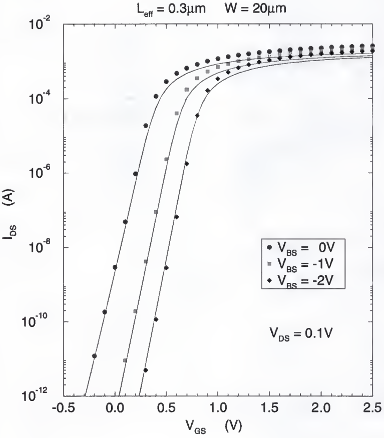

Figure 4.13 Subthreshold plot with $V_{BS} \neq 0V$ using Level = 3 model parameters.

4.5.3 Calibration Based on Strong-Inversion Characteristics

In strong inversion, the model parameters which can be evaluated are **UO**, **THETA**, **THETA2**, **RDS** and **VSAT**. If an LDS/LDD is present, **LLDD** and **NLDD** can also be evaluated here. For all structures, it is assumed that the parasitic source and drain resistances are equal (and so are L_{LDS} and L_{LDD}) due to symmetry.

At low V_{DS}, the linear region characteristics of the MOSFET are similar to that of a resistor with its total ON resistance (R_{ON}) given approximately by

$$R_{ON} \equiv \frac{V_{DS}}{I_{DS}} \cong \frac{\mathbf{RDS}}{W} + \frac{L_{eff}}{WC_{ox}(V_{GS} - V_T)\mu(\mathbf{UO}, \mathbf{THETA}, \mathbf{THETA2})}. \qquad (4.5)$$

As can be seen from (4.3), R_{ON} is dependent on **UO**, **THETA**, **THETA2** and **RDS**. To isolate the effects of **RDS** from those of **UO/THETA/THETA2**, it can be shown from (4.5) that g_m/I_{DS}^2 is nearly independent of **RDS**. This allows us to first evaluate **UO**, **THETA** and **THETA2** to fit the g_m/I_{DS}^2 characteristics, independent of **RDS**. Once these three parameters are tuned, **RDS** can be explicitly calibrated from (4.5). If an LDS/LDD is present in the structure, **LLDD** is set equal to the spacer width as defined by technology, and **NLDD** is set to roughly correspond to the LDD dose. Typically the LDD doping is in the $\text{mid} - 10^{18}\ \text{cm}^{-3}$ range. When an LDS/LDD is present the resistance **RDS** in (4.5) would include implicitly the ohmic component of the series resistance (**2*RLDD**). However, the **RDS** in the model card is the source/drain parasitic resistance without **RLDD**. Hence, **2*RLDD** must be subtracted off from the evaluated (total) **RDS**. Note that if, as in some technologies, the LDS/LDD is more of a source/drain extension, then the effect of the LDS/LDD is to simply increase the total resistance **RDS** and the non-ohmic drops in the LDD will not be important. For such cases, it is recommended that the LDS/LDD feature be turned off in the model to speed up run time. The extraction technique for **RDS** described above should then be carried out as though there were no LDS/LDD. After evaluating these parameters (Level = 4 in Table 4.4), the resulting threshold plot is Figure 4.14.

At high V_{DS}, and relatively large V_{GS}, the current saturates in short-channel MOSFETs due to carrier velocity saturation. From the model formalism, the current for a short-channel device in strong inversion at high V_{DS} is

$$I_{DS} \cong \frac{W\mu_{eff}}{2(C_{ox}' + C_d)L_{eff}} \frac{\left[Q_c^2(0) - \left(\frac{I_{DS}}{WVSAT}\right)^2\right]}{\left[1 + \frac{\mu_{eff}}{2VSATL_{eff}} V_{DS(sat)}\right]} . \qquad (4.6)$$

From (4.6) and the output I_{DS}-V_{DS} characteristics, **VSAT** can be evaluated at V_{DS} close to $V_{DS(sat)}$ the saturation drain voltage at moderately high V_{GS}. (The initial guess for **VSAT** can be set to 6×10^6 cm/s for NMOS although 1×10^7 cm/s was used in order to be consistent with MEDICI.) The final parameter set (Level = 5 in Table 4.4) results in the linear-saturation characteristics of Figure 4.15.

At high V_{DS}, the current saturates in long-channel MOSFETs due to carrier pinch-off at the drain end. From the model formalism, the current for a long-channel device in strong inversion at high V_{DS} is

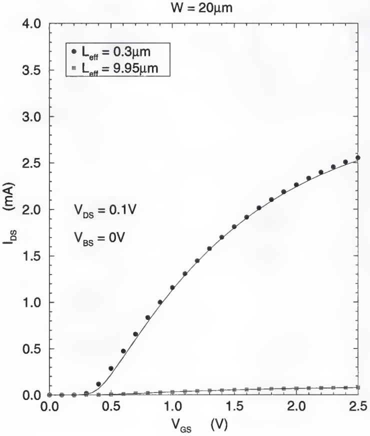

Figure 4.14 Threshold plot with $V_{BS} = 0V$ using Level = 4 model parameters.

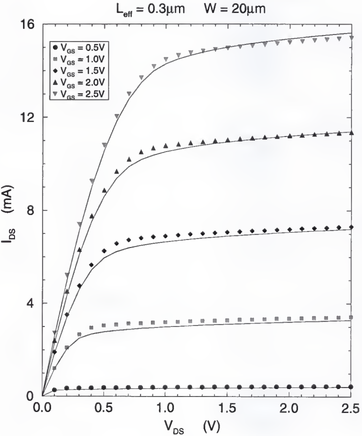

Figure 4.15 Linear-saturation plot with V_{BS} = 0V using Level = 5 model parameters.

$$I_{DS} \cong \frac{W\mu_{eff}}{L_{eff}} \frac{Q_c^2(0)}{2(C_{ox}' + C_d)}. \tag{4.7}$$

From (4.7) and the long-channel output I_{DS}-V_{DS} characteristics, the values of **XLH** and **NBH** which both affect C_d can be further tuned from the values obtained in the subthreshold region of operation.

4.5.4 Short-Channel Effects Parameter

In scaled devices, the short-channel effects significantly affect the device output characteristics. A single parameter is available to tune the average short-channel effects (**FCS**). **FCS** controls the $V_{DS} = 0$ short-channel effects and should be tuned in the low-drain bias subthreshold region for a minimum channel length device. This parameter accounts for the non-parabolic potential which was assumed in deriving an expression for the two-dimensional effects.

4.5.5 Reverse Short-Channel Effect Parameters

In scaled devices, it is also necessary to account for nonuniform lateral doping profiles due to halos and also the Reverse Short-Channel Effect (RSCE). This is accounted for by using a lateral doping transform which assumes quasi-Gaussian profiles (with peak doping of N_o and a characteristic length y_o) near the source/drain junctions modify the surface doping concentration as a function of the channel length [Bru95]. The two parameters associated with this effect should be tuned to the threshold voltages of two short-channel devices showing RSCE.

4.6 Application to Simulated 0.35μm Technology

4.6.1 0.35μm Technology

With the UFET MMSPICE/API implementations, verification is provided by comparing subthreshold, threshold and linear-saturation characteristics over different channel lengths and substrate biases with numerical simulations using MEDICI. For the verification, the parameters evaluated in Section 4.5 are used, and it should be stressed that no attempt was made to find the optimal values for the parameters. It is also important to note that the same parameters are used for all simulation results shown in this section without "tweaking" to give the best results for each individual figure.

4.6.2 DC Verification

The low-V_{DS} behavior is exhibited in the threshold plot of Figure 4.16 and the subthreshold plot shown in Figure 4.17 with no substrate bias. With parameters tuned from the 0.3μm and 10μm devices in Figure 4.5, the model accurately predicts the channel length and V_{GS} dependence of the channel current for channel lengths ranging from long to shorter than the target length (0.3μm) for which the technology is designed. The V_{BS} dependence of the model is shown in Figures 4.18 and 4.19 for the nominal channel length of the technology. The channel current is accurately modeled in all regions of operation by accounting for the increased doping in the p^+ region along the channel, and UFET also shows a continuous transconductance result in Figure 4.20. The discrepancies in the V_{BS} plots can be attributed to the different mobility models used in MEDICI and UFET, and the transconductance errors are

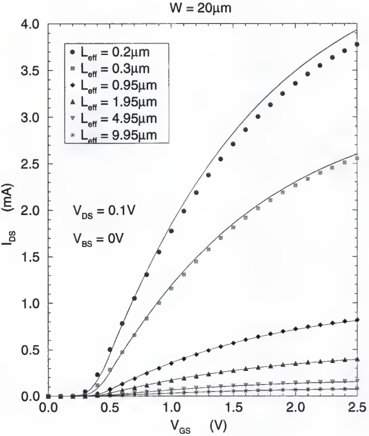

Figure 4.16 Threshold plots of UFET-(lines) and MEDICI-(points)simulated data for V_{BS} = 0V showing channel length dependence.

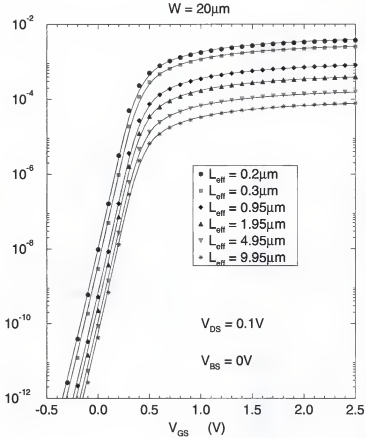

Figure 4.17 Subthreshold plots of UFET-(lines) and MEDICI-(points)simulated data for V_{BS} = 0V showing channel length dependence.

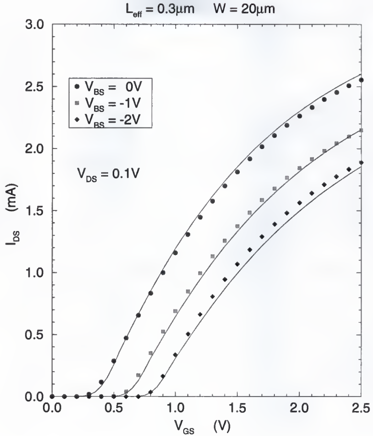

Figure 4.18 Threshold plots of UFET-(lines) and MEDICI-(points)simulated data for L_{eff} = 0.3μm showing V_{BS} dependence.

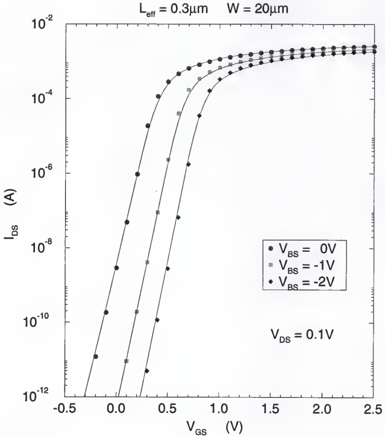

Figure 4.19 Subthreshold of UFET- and MEDICI-simulated data plot for L_{eff} = 0.3μm showing V_{BS} dependence.

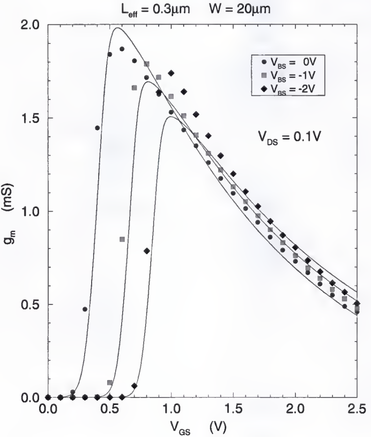

Figure 4.20 Transconductance plots of UFET-(lines) and MEDICI-(points)simulated data for L_{eff} = 0.3μm showing V_{BS} dependence.

what result from the parameter evaluation. In order to better model the transconductance, the mobility parameters (**UO**, **THETA1** and **THETA2**) should be evaluated from a transconductance plot. The V_{DS} dependence of the model is shown in Figure 4.21. The channel current is well modeled for both the long- and short-channel cases for low and high drain biases. The long-channel device shows no drain-induced effects as expected, and the short-channel device shows significant effects from DIBL in the subthreshold region of operation. The error in the subthreshold slope for the short-channel device at high drain bias can be attributed to deviations from the assumed parabolic potential used to define the two-dimensional effects.

The long-channel linear-saturation characteristics shown in Figure 4.22 clearly shows the pinch-off behavior of the channel current of the device for all gate biases. The model gives good fits to the MEDICI data since the non-fundamental parameters such as the saturated drift velocity and the mobility dependence on lateral field only play a minor part in determining the output characteristics of this long-channel device. The significant error the long-channel device is due to the assumption of a constant depletion capacitance along the channel to account for the depletion charge variation. In a long-channel device controlled by pinch-off, this assumption tends to under-predict the saturation current, and the magnitude of the error is dependent on well the actual doping profile tends to keep the depletion capacitance constant along the channel. For the nominal channel length device shown in Figure 4.23, the effect of channel length modulation due to the applied drain bias is clearly evidenced by the increase in the drain conductance $\left(g_{ds} \equiv \frac{dI_{CH}}{dV_{DS}}\right)$ as

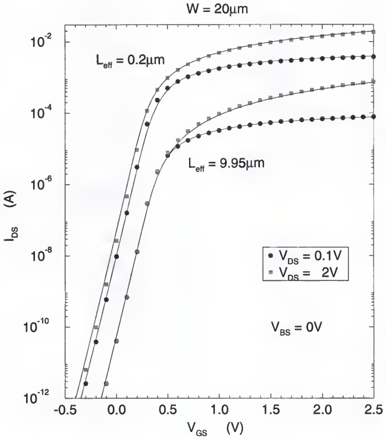

Figure 4.21 Subthreshold plots of UFET-(lines) and MEDICI-(points)simulated data for V_{BS}=0V showing DIBL.

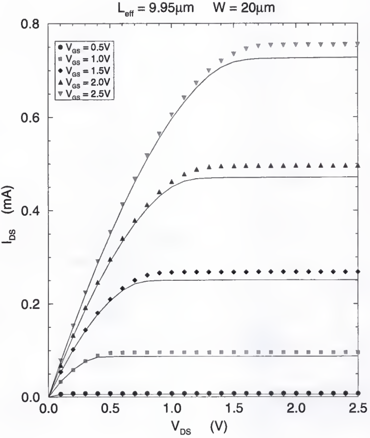

Figure 4.22 Linear-saturation plots of UFET-(lines) and MEDICI-(points)simulated data for $L_{eff} = 9.95\mu m$ with $V_{BS} = 0V$.

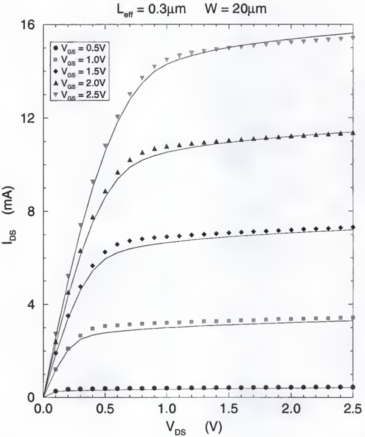

Figure 4.23 Linear-saturation plots of UFET-(lines) and MEDICI-(points)simulated data for $L_{eff} = 0.3\mu m$ with $V_{BS} = 0V$.

compared to the long-channel case. There is a good fit for the channel current with some error in the drain conductance, for which there is no parameter in the model as shown in Figure 4.24. The likely cause for the error in the drain conductance is the **DL** assumed for the devices in this technology. Since the technology was simulated with MEDICI, the **DL** was assumed to represent the difference between the physical gate length and the metallurgical channel length, but a recent paper [Niu97] indicates that the effective (i.e., gate-controlled) channel length is larger than the metallurgical channel length suggesting that **DL** should be smaller than the value used. This will decrease the drain conductance while necessitating an increase in **VSAT** which tends to be different from the MEDICI value due to the differing mobility models used. This dependence of drain conductance on **DL** implies the possibility that **DL** should be tuned to best fit the drain conductance if this does not compromise the model accuracy in other regions of operation.

4.6.3 Charge Model Verification

The DC portion of the model has been validated against MEDICI simulations, but the new charge modeling must now be verified. The charge model is qualitatively verified by looking at the intrinsic capacitances and trans-capacitances in both long and short-channel devices. These intrinsic capacitances are defined by the following relationships.

$$C_{ij} \equiv \begin{cases} -\dfrac{\partial Q_i}{\partial V_j} & i \neq j \\ \dfrac{\partial Q_i}{\partial V_j} & i = j \end{cases} \tag{4.8}$$

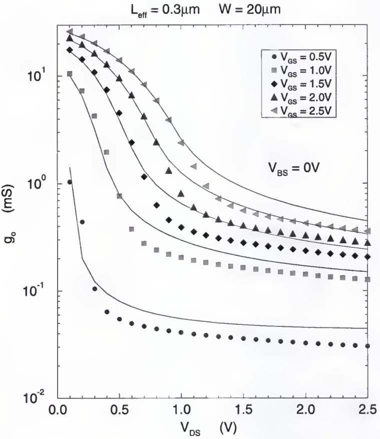

Figure 4.24 Drain conductance plots of UFET-(lines) and MEDICI-(points)simulated data for L_{eff} = 0.3μm.

The UFET intrinsic gate capacitances for a long-channel device are shown in Figure 4.25. Notice the smooth transitions between the different regions of operation, i.e., accumulation/depletion, subthreshold/threshold and linear/saturation, that result from the C_{∞} continuity of the model. The long-channel strong-inversion transcapacitances (see Figure 4.26) also show the same smooth transition across the linear/saturation boundary, and the gate and bulk transcapacitances are symmetric with respect to the source and drain for $V_{DS} = 0$ as expected. The UFET capacitance curves show good qualitative and quantitative agreement with the corresponding results from MEDICI presented in Figures 4.27 and 4.28.

The UFET intrinsic gate capacitance and transcapacitances for the short-channel device are shown in Figures 4.29 and 4.30, and they still exhibit smooth transitions between the different regions of operation. The model correctly predicts the differences in the capacitance resulting from decrease in channel length. The simulation results of Figure 4.29 show the effect of DIBL in weak inversion, and they also exhibit the expected velocity saturation characteristics in strong inversion as opposed to the pinch-off behavior of a long-channel device. As in the long-channel case, there is still good qualitative agreement between the UFET capacitances and the MEDICI results shown Figures 4.31 and 4.32. The quantitative error in the short-channel devices is due to the overlap (parallel plate) and fringing (neglected) capacitance modeling in UFET. The effect of DIBL on the gate capacitance is also over predicted which is due to the assumption of the parabolic potential along the channel to define the two-dimensional effects.

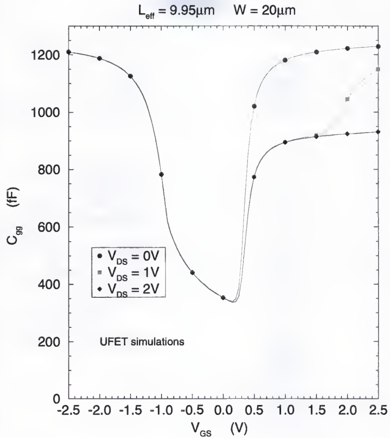

Figure 4.25 UFET-simulated gate capacitance for $L_{eff} = 9.95\mu m$ with $V_{BS} = 0V$.

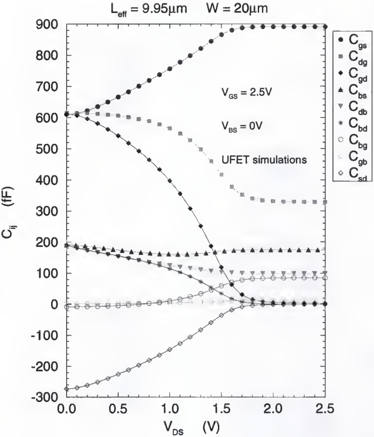

Figure 4.26 UFET-simulated transcapacitances for L_{eff} = 9.95μm with V_{BS} = 0V.

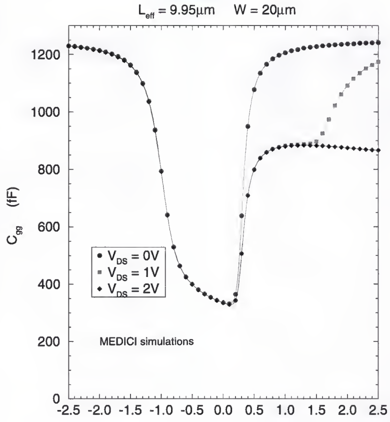

Figure 4.27 MEDICI-simulated gate capacitance for L_{eff} = 9.95μm with V_{BS} = 0V.

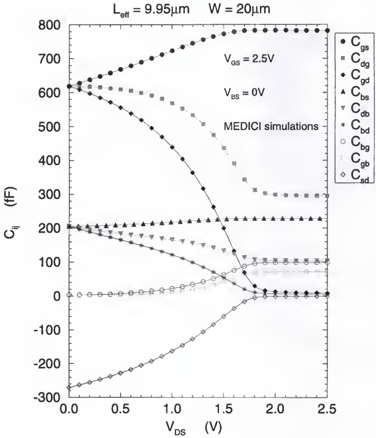

Figure 4.28 MEDICI-simulated transcapacitances for L_{eff} = 9.95μm with V_{BS} = 0V.

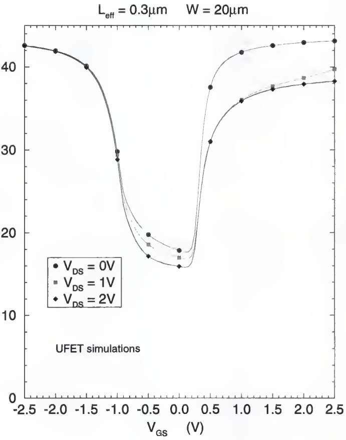

Figure 4.29 UFET-simulated gate capacitance for $L_{eff} = 0.3\mu m$ with $V_{BS} = 0V$.

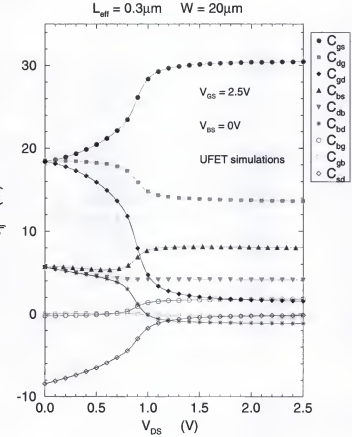

Figure 4.30 UFET-simulated transcapacitances for $L_{eff} = 0.3\mu m$ with $V_{BS} = 0V$.

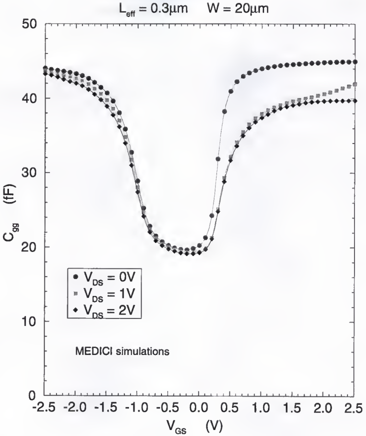

Figure 4.31 MEDICI-simulated gate capacitance for $L_{eff} = 0.3\mu m$ with $V_{BS} = 0V$.

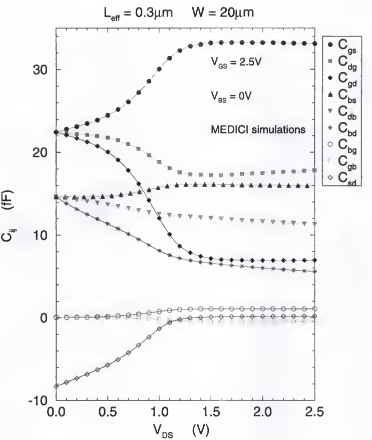

Figure 4.32 MEDICI-simulated transcapacitances for L_{eff} = 0.3μm with V_{BS} = 0V.

Although MEDICI does not account for quantum mechanical effects and polysilicon-gate depletion was not included in the simulations, the impact of these two effects on the gate capacitance curves can be shown by UFET. In Figure 4.33, the three curves represent the gate capacitance without polysilicon-gate depletion or quantum mechanical effects, with polysilicon-gate depletion and with polysilicon-gate depletion and quantum mechanical effects. Neither of these effects significantly influences the results in weak-inversion, but both tend to increase the threshold voltage and reduce the capacitance in strong inversion. The quantum mechanical effects in the accumulation layer also lead to a reduction in the gate capacitance below flatband similar to the strong inversion results.

4.7 Application to 0.25μm Technology

An Semiconductor Research Corporation (SRC) member company provided measured data from a 0.25μm technology (K. Stiles, private communication, 1997) still in the design stage. This technology has a 5nm gate oxide with an LDD/LDS structure designed for a 2.5V supply. Since the process was still under design with the previous generation of equipment, the process control of ΔL as a function of channel length was poor (as reported by the company). Some liberty was assumed in tuning the parameters which resulted in a reasonable fit for the longer channel devices (as shown in Figure 4.34), but the physical significance of the parameters was compromised by this process. The significant problems seen in the subthreshold plot are due to assuming that DL was a constant, and the preliminary accounting for RSCE/halo effects as presented in Chapter 3. Due to this problem, effort was focused solely on the long-channel device, and the only other results

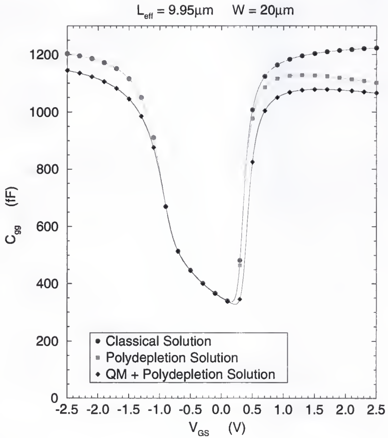

Figure 4.33 UFET-simulated impact of polysilicon-gate depletion and quantum mechanical effects on gate capacitance.

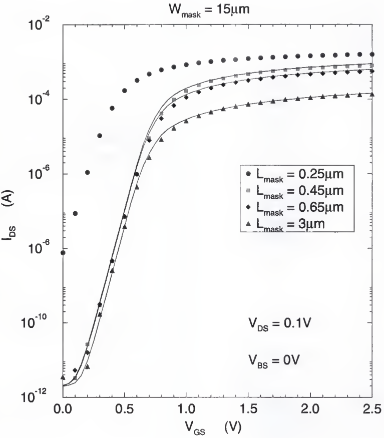

Figure 4.34 Subthreshold plot of UFET-simulated (lines) and measured (points) data in 0.25μm technology.

presented are for this channel length. UFET was able to accurately predict the both the body effect (shown in Figure 4.35) and the drain bias characteristics off Figure 4.36. As in the simulated 0.35μm technology, the source of the error in the drain bias plot is due to the constant depletion capacitance assumption. In addition, the company also supplied data taken over a range of temperatures, which allowed the evaluation of the temperature dependencies in the model. The results shown in Figure 4.37 validate the temperature modeling in UFET, and the discrepancies seen at the lower temperatures may be due measurement problems (K. Stiles, private communication, 1997).

4.8 Application to 0.15μm Technology

4.8.1 0.15μm Technology Parameters

Measured data was supplied by an SRC member company (Y. Taur, private communication, 1997) from their aggressive 0.15μm retrograde technology with a 27Å gate oxide, LDD/LDS structures having a peak doping of 8×10^{19} cm^{-3}, a peak channel doping of 1×10^{18} cm^{-3} and halo implants processed using x-ray lithography. Unfortunately, the measured data provided shows signs of pervasive contact problems and device-to-device variations. Due to the contact resistance problem, the parameters were tuned from the 0.175μm and 10μm devices, and the 0.15μm device was modeled by varying only the parasitic source/drain resistance.

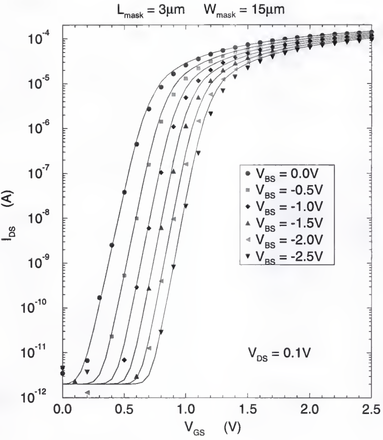

Figure 4.35 Subthreshold plot of UFET-simulated (lines) and measured (points) data in 0.25µm technology showing body effect.

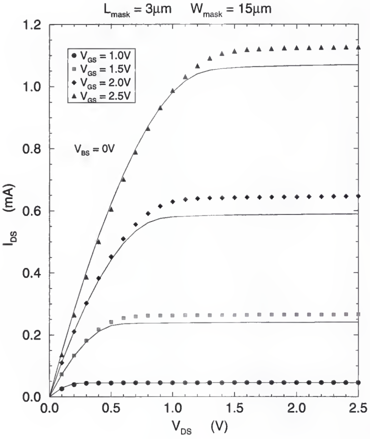

Figure 4.36 Linear-saturation plot of UFET-simulated (lines) and measured (points) data in 0.25µm technology.

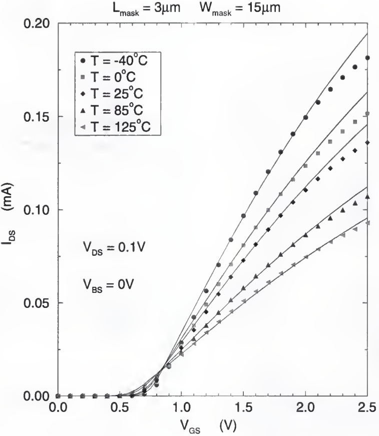

Figure 4.37 Threshold plot of UFET-simulated (lines) and measured (points) data in 0.25μm technology showing temperature effects.

4.8.2 Verification

The resulting subthreshold plots are shown in Figure 4.38 with the subthreshold slope tuned to the value just below threshold. Although the results for the long-channel devices are reasonable, the short-channel devices show significant discrepancies. These discrepancies can be attributed to the onset of punch-through current and to the simple model being used to model RSCE/halo effects. The threshold plot of Figure 4.39 shows that UFET is able to model the characteristics of the measured devices in a deep-submicron technology for the long-channel devices. However, the RSCE/halo effects cause a shift in the threshold voltage which is not well predicted by UFET, indicating that the RSCE/halo model in UFET does not completely account for this effect. (Note that the errors in the channel current for the longer channel devices are within the 10% variation seen between adjacent devices with the same W/L.) The drain-induced effects are shown in Figure 4.40 show an increased error in subthreshold slope and current due to RSCE/halo effects and possible punch-through current at the higher drain bias. The drain bias characteristics of a long- and short-channel device are shown in Figures 4.41 and 4.42 respectively. Here, the long-channel device shows significant error (~15%) which can again be attributed to the model assumption of a constant depletion capacitance along the channel. The error in the short-channel device can be attributed to velocity overshoot (~10% [Jan97]) which is not modeled and to possible errors in tuning the value of **DL**. The charge modeling has also been further verified with the measured gate capacitance of a long-wide device as shown in Figure 4.43. Note that the capacitance is predicted well by UFET calibrated only via DC data.

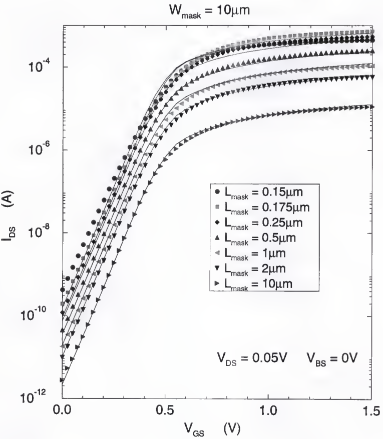

Figure 4.38 Subthreshold plot of UFET-simulated (lines) and measured (points) data in 0.15μm technology.

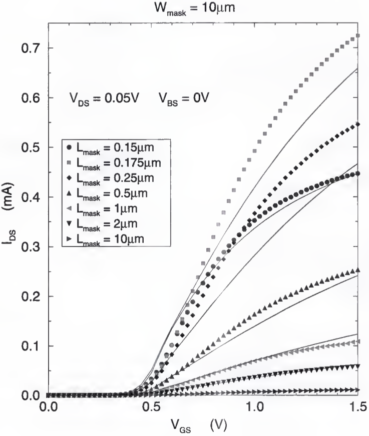

Figure 4.39 Threshold plot of UFET-simulated (lines) and measured (points) data in 0.15μm technology.

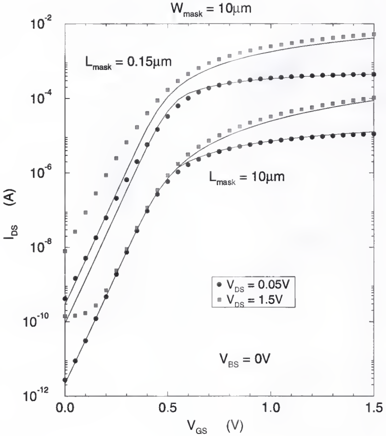

Figure 4.40 Subthreshold plot of UFET-simulated (lines) and measured (points) data in 0.15μm technology showing the drain-induced effects.

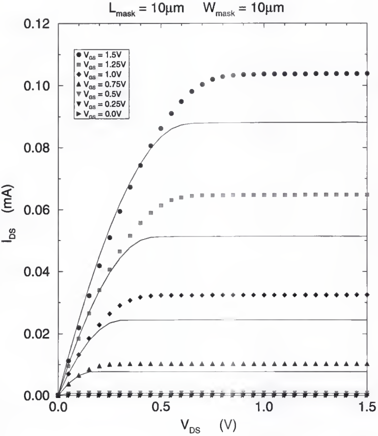

Figure 4.41 Linear-saturation plot of UFET-simulated (lines) and measured (points) data in 0.15µm technology for L = 10µm.

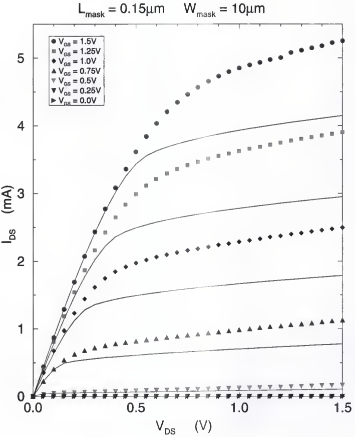

Figure 4.42 Linear-saturation plot of UFET-simulated (lines) and measured (points) data in 0.15μm technology for L = 0.15μm.

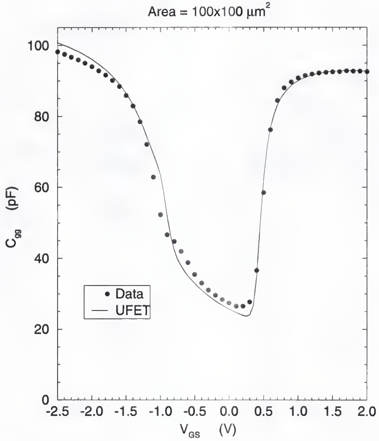

Figure 4.43 Gate Capacitance plot of UFET-simulated (line) and measured (points) data in 0.15μm technology for a long-wide device.

The discrepancies in the low-V_{DS} plots in this 0.15μm technology are due to the Reverse Short-Channel Effect and the presence of a halo. The preliminary accounting in UFET for these effects, which are important in scaled technologies, is being done using a model first developed for threshold voltage. This accounting for RSCE/halo fails to model this dependence properly, and this is an area for further review (see Chapter 6). The discrepancies in the drain characteristics seen in the long-channel device can be attributed to the assumption of a constant depletion capacitance along the channel. Although this assumption was valid for the two other technologies discussed, it breaks down for this 0.15μm technology. This indicates that the retrograde doping profile may not be as steep in this technology which allows the depletion depth to vary more along the channel increasing the current drive in long-channel devices where pinch-off controls the characteristics. The need for an accounting of velocity overshoot also needs to be investigated although "clean" data would be needed for this. As an initial assessment of this effect, hydrodynamic simulations should be run using MEDICI to investigate the impact of velocity overshoot in extremely scaled devices with regard to the UFET formalism.

4.9 Conclusion

The new UFET model was verified against MEDICI simulations and measured data for the DC channel current across all biases and channel lengths with (overall) good results. The charge modeling was also verified through the intrinsic capacitances for both long- and short-channel devices across all biases with quantitative verification of the gate charge model. The model is useful not only for digital design, but also for analog design where the derivatives of the output characteristics are important. The limited number of physical, process-based model parameters with inherent correlation between the parameter values and device characteristics also make the model ideally suited for process design/integration and statistical simulations.

CHAPTER 5
MEDICI BENCHMARK AND A SENSITIVITY STUDY

5.1 Introduction

Two important issues for any device model are parameter extraction/ evaluation and correlation to process parameters as needed for process design/ integration, statistical simulations and sensitivity analyses. In models such as BSIM3v3 with a large number of parameters, a copious amount of data across several channel lengths and all terminal biases is needed in order to extract the parameters controlling the length and bias dependencies. As a result of the excessive optimization needed for such models, the correlation between model parameters and process variations may not be clear, may be spread across several parameters or may not exist at all. With its small number of physical parameters, the process-based UFET model makes parameter evaluation relatively easy as demonstrated in Chapter 4 while maintaining a strong correlation to process variations.

In this chapter, UFET is first applied to a simulated 0.1μm technology to demonstrate its applicability to extremely scaled technologies. Based on only DC calibration involving minimal data, transient and AC figures of merit are simulated, and their sensitivities are examined. A circuit application is then presented using the 0.15μm technology in Chapter 4 to demonstrate the UFET's utility in circuit sensitivity analyses.

5.2 MEDICI Benchmark

In order to further demonstrate the utility of this new process-based model, a 0.1μm technology was simulated using MEDICI, and the UFET parameters were tuned using a limited set of DC data from two, short- and long-channel (L = 0.1μm and 10μm), devices over a limited range of terminal biases:

- I_{CH}-V_{GS} for V_{DS} = 0.1V and V_{DD}
- I_{CH}-V_{DS} for V_{GS} = 0.5V, 1.0V and 1.5V
- I_{CH}-V_{GS} for V_{DS} = 0.1V and V_{BS} = 0V and -1.5V

Trying to use a model such as BSIM3v3 for this exercise is problematic, if not impossible, due to the copious amounts of data required for the intensive optimization required for parameter-extraction (K. R. Green, private communication, 1997). After tuning the model parameters, UFET- and MEDICI-simulated results were compared for two intermediate channel lengths (L = 0.3μm and 1μm) over the same range of terminal biases. In addition, transient and AC simulations were done with MEDICI and UFET to find the intrinsic propagation delay (t_{pd}) and cutoff frequency (f_T) of the four devices. In order to show the physical nature of the model, sensitivity simulations were performed with assumed variations in t_{ox} and ΔL from the nominal values to assess the impact on device performance.

5.2.1 0.1μm Technology

The technology was designed to achieve a 0.5V threshold voltage with minimal threshold voltage roll-off due to charge-sharing and drain induced effects. Based on published 0.1μm technologies [Iwa93, Mii94], the gate oxide was chosen to be 5nm with a substrate doping of 7×10^{17} cm^{-3}, a junction depth of 0.08μm corresponding to the extrinsic source/drain junction depth and a gate overlap of 0.015μm due to the lateral diffusion of the source and drain junctions. The peak doping was set at 2×10^{18} cm^{-3} with a Gaussian profile near the surface determined by the threshold voltage criterion. In order to reduce simulation time several simplifications/assumptions were made about the device structure:

- The contact resistance was assumed to be zero.
- The polysilicon-gate doping was assumed to be large, i.e., no polysilicon-gate depletion effect.
- The lateral doping profile was assumed to be uniform, i.e., no RSCE.
- The simulation was done using only drift-diffusion variables, i.e., no velocity overshoot.

Since the device simulations were done using an older version of MEDICI, the quantum mechanical effects were not included in this benchmark. A summary of the technology and simulation parameters is shown in Table 5.1.

5.2.2 DC Results

After the DC MEDICI simulations were completed, the model parameters were tuned with the 0.1μm and 10μm devices using the procedure outlined in Chapter 4, and this set of model parameters was then used to predict the 0.3μm and 1μm device characteristics. Note that although the model parameters were evaluated using only the 0.1μm and 10μm devices, the results are presented using all four channel lengths in some of the figures to follow.

Table 5.1 Nominal 0.1μm Technology

Parameter	Value
t_{ox}	5nm
X_j	0.08μm
ΔL	0.03μm
Substrate Doping	$7\times10^{17}\ cm^{-3}$
Peak Doping	$2\times10^{18}\ cm^{-3}$
V_{DD}	1.5V
$V_t(V_{DS} = 0.1V)$	0.5V
Reverse Short-Channel Effect	No
Polysilicon-gate Depletion	No
LDD	No
Contact Resistance	No
Hydrodynamic Simulation	No
Quantum Mechanical Effect	No

In the low-V_{DS} subthreshold plot of Figure 5.1, UFET accurately models the subthreshold slope and current of all four channel lengths with no substrate bias. UFET also models the behavior above threshold as shown in Figure 5.2 again with no substrate bias and $V_{DS} = 0.1V$. The effects of the drain bias on the different channel lengths are presented in Figure 5.3. The long-channel device shows no drain-induced effects as expected, and the DIBL effects in the subthreshold region of operation increase as the channel length becomes smaller. There is good agreement between the UFET- and MEDICI-predicted results with no tuning of the DIBL effect for the intermediate channel lengths. The DIBL effect in the 0.3μm device are over-predicted which may mean that the drain-induced effects tend to diminish faster than the $\frac{1}{L^2}$ dependence in the model derived by assuming a parabolic potential for the analysis of the two-dimensional effects.

The body effect is shown in Figures 5.4-5.7, and there is good agreement for the three longest channel lengths between MEDICI and UFET. However, the MEDICI results for the 0.1μm device show an error due to the severe two-dimensional effects in this device due to the overlapping source and drain depletion regions (which was later verified using MEDICI). This implies that the technology is not optimally designed since punch-through would occur at higher drain biases, but it is important to note that UFET was still able to predict the short-channel effects until the overlapping depletion regions completely dominated the characteristics.

The drain characteristics are shown in Figures 5.8-5.11 with good agreement (less than 10% error for the intermediate channel lengths) between UFET

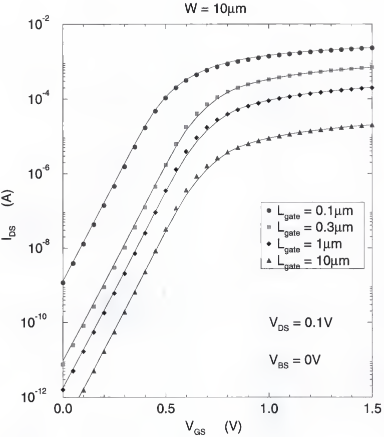

Figure 5.1 Subthreshold plots of UFET-(lines) and MEDICI-(points)simulated data in nominal 0.1μm technology.

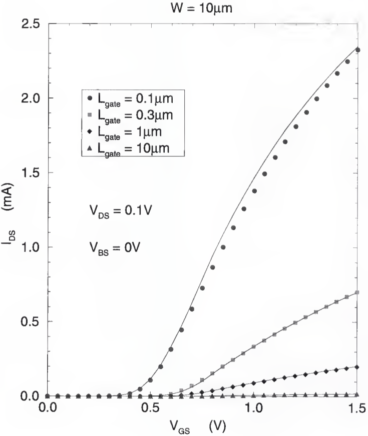

Figure 5.2 Threshold plots of UFET-(lines) and MEDICI-(points)simulated data in nominal 0.1μm technology.

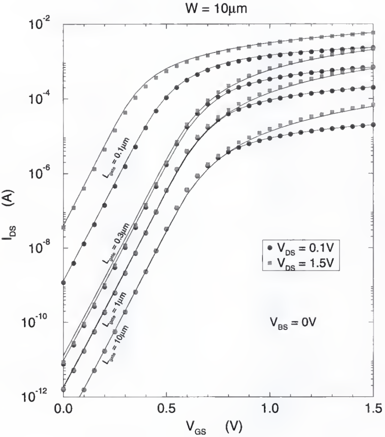

Figure 5.3 Subthreshold plots of UFET-(lines) and MEDICI-(points)simulated data in nominal 0.1μm technology showing DIBL.

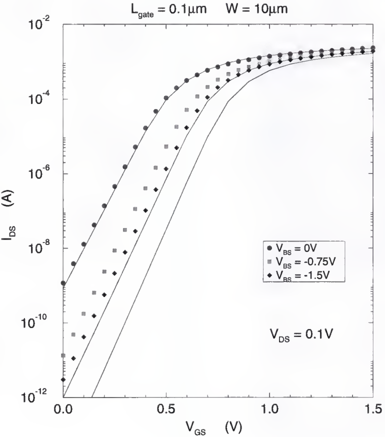

Figure 5.4 Subthreshold plots of UFET-(lines) and MEDICI-(points)simulated data in nominal 0.1μm technology for L = 0.1μm showing V_{BS} dependence.

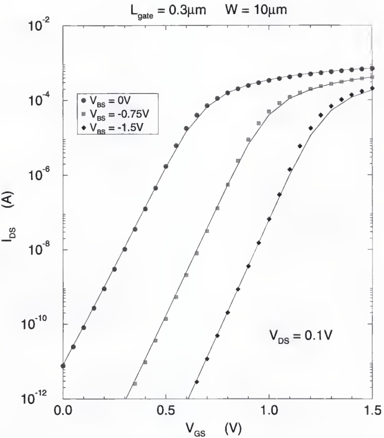

Figure 5.5 Subthreshold plots of UFET-(lines) and MEDICI-(points)simulated data in nominal 0.1μm technology for L = 0.3μm showing V_{BS} dependence.

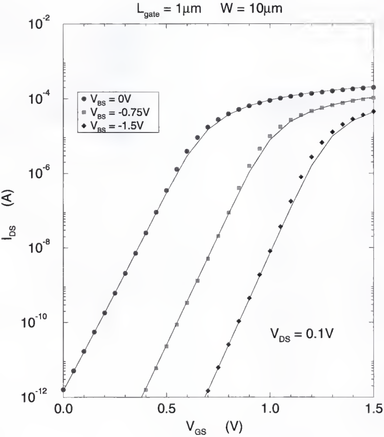

Figure 5.6 Subthreshold plots of UFET-(lines) and MEDICI-(points)simulated data in nominal 0.1μm technology for L = 1μm showing V_{BS} dependence.

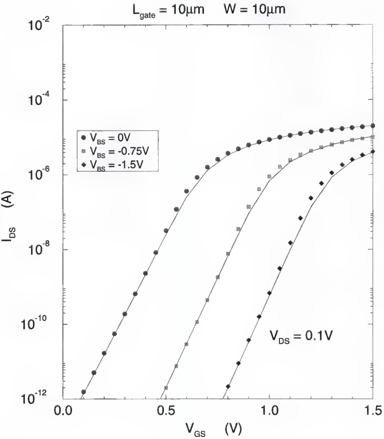

Figure 5.7 Subthreshold plots of UFET-(lines) and MEDICI-(points)simulated data in nominal 0.1μm technology for L = 10μm showing V_{BS} dependence.

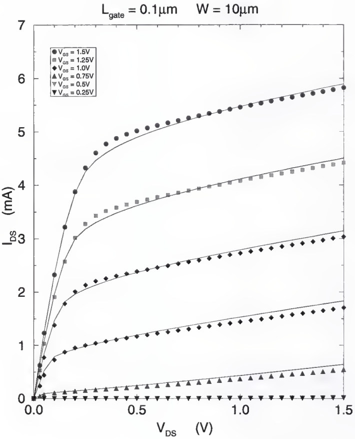

Figure 5.8 Triode-Saturation plots of UFET-(lines) and MEDICI-(points)simulated data in nominal 0.1μm technology for L = 0.1μm.

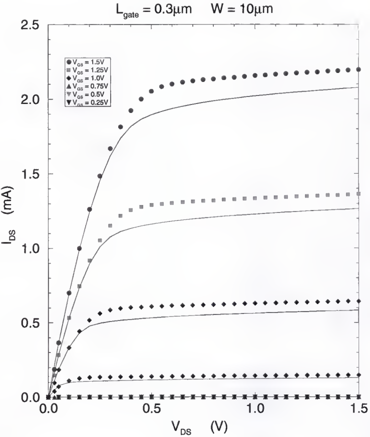

Figure 5.9 Triode-Saturation plots of UFET-(lines) and MEDICI-(points)simulated data in nominal 0.1μm technology for L = 0.3μm.

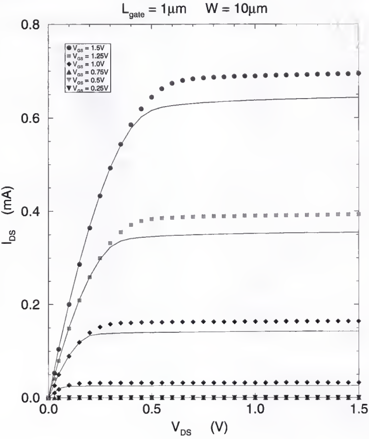

Figure 5.10 Triode-Saturation plots of UFET-(lines) and MEDICI-(points)simulated data in nominal 0.1μm technology for L = 1μm.

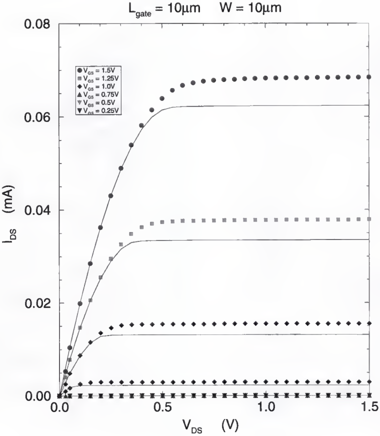

Figure 5.11 Triode-Saturation plots of UFET-(lines) and MEDICI-(points)simulated data in nominal 0.1μm technology for L = 10μm.

and MEDICI. There is a good match for the channel current with only a small error in the drain conductance for the 0.1µm device. As was the case for the 0.35µm technology, the likely cause for the error in the drain conductance is the **DL** assumed. Since the technology was simulated with MEDICI, the **DL** was assumed to represent the difference between the physical gate length and the metallurgical channel length, but a recent paper [Niu97] indicates that the effective (i.e., gate-controlled) channel length is larger than the metallurgical channel length, suggesting that **DL** should be smaller than the value used. This will decrease the drain conductance while necessitating an increase in **VSAT** which tends to be different from the MEDICI value due to the differing mobility models used. The increase in VSAT will tend to decrease the error seen in the 0.3µm device. For the 1µm and 10µm devices, the dominant source of error is the constant depletion capacitance approximation used.

5.2.3 Transient and AC Results

In order to demonstrate the predictive nature of UFET in a digital simulation, the gate delay of the devices was investigated. Due to limitations in the simulation capabilities of generic MEDICI (i.e., without the Circuit Analysis Advanced Application Module), only the intrinsic pull-down delay of the devices was simulated as shown in Figure 5.12. Also due to the poor time-step control which required the use of a small constant time-step in these simulations, the intrinsic delay of the 10µm devices was not simulated. As shown in Figure 5.13, UFET accurately predicts the channel length and supply voltage dependencies of the intrinsic delay for the three different channel lengths. The slight differences between the MEDICI and

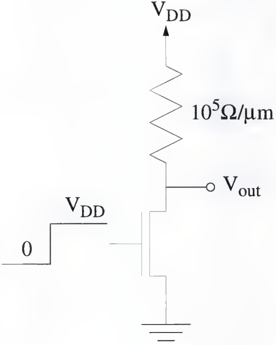

Figure 5.12 Intrinsic delay circuit.

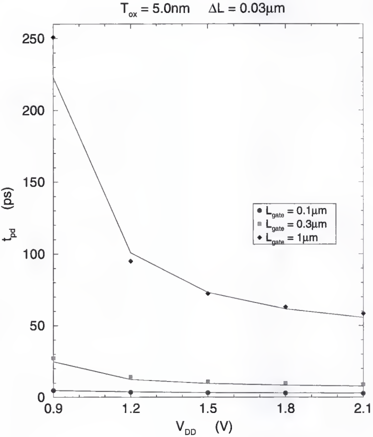

Figure 5.13 UFET-(lines) and MEDICI-(points)simulated intrinsic pull-down delay in nominal 0.1μm technology.

UFET results can be explained by the differences in saturated channel currents seen in Figures 5.8-5.11.

Application of UFET for analog design requires verification of the (derivatives of the) channel current and terminal charges. This has been done by simulating the cutoff frequency [Gra93],

$$f_T \cong \frac{1}{2\pi}\frac{g_m}{C_{GG}}, \qquad (5.1)$$

with both MEDICI and UFET. In Figure 5.14, the cutoff frequency is shown as a function of both channel length and gate bias, and UFET accurately predicts both trends. The maximum cutoff frequency, which occurs at approximately $g_{m(max)}$ as can be seen in (5.1), can be extracted from the data in Figure 5.14 and plotted as a function of channel length as shown in Figure 5.15. UFET is able to accurately model the cutoff frequency over two orders of magnitude in channel length.

The results for the intrinsic delay and cutoff frequency were obtained using the parameter set calibrated from limited DC data. This shows the predictability of UFET, which has practical applications in assessing preliminary data from new technologies. The physical nature of the model parameters also allows UFET to be used in investigations of device sensitivity to process variations as will now be demonstrated.

5.2.4 Device Sensitivity

As both vertical and lateral device dimensions continue to shrink, it is becoming even more important to tightly control the fabrication process in order to

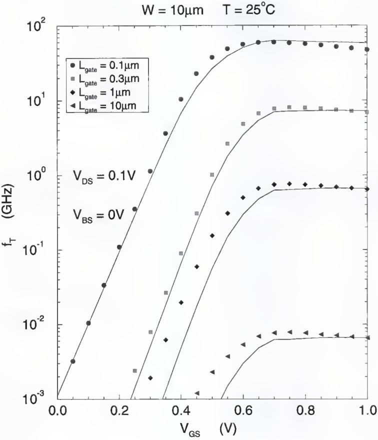

Figure 5.14 UFET-(lines) and MEDICI-(points)simulated cutoff frequency in nominal 0.1μm technology.

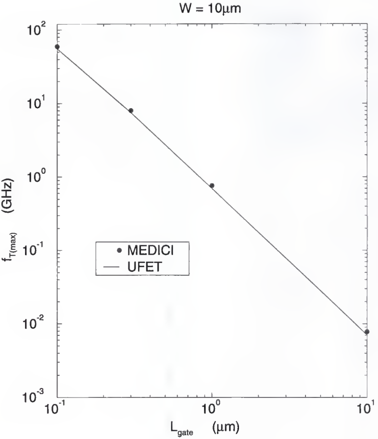

Figure 5.15 UFET-(line) and MEDICI-(points)simulated cutoff frequency in nominal 0.1μm technology.

minimize device variations across lots (to improve yield) and also wafers (in order to ensure the device matching needed in some circuits). At the device level, sensitivity to variations in oxide thickness and lateral diffusion (ΔL) can be easily shown using the process-based model parameters in UFET.

The oxide thickness was assumed to have a maximum 10% variation which is consistent with published variations [Aro95]. For the case of pull-down delay, the variation in oxide thickness is a first-order effect due to the linear variation in drive current with t_{ox}. As shown in Figures 5.16 and 5.17, UFET models the increase and decrease in the pull-down delay associated with the change in t_{ox}. The cutoff frequency as given by (5.1) is independent of t_{ox} to first-order, and the resulting plots of f_T in Figure 5.18 show the device has little sensitivity to variations in the oxide thickness.

Assuming a typical variation in ΔL of 50% [Aro95], sensitivity simulations of t_{pd} and f_T were performed. As expected from a simple drive current analysis, the variation of the pull-down delay is greatest for short-channel devices with almost no sensitivity in the long-channel case as shown in Figures 5.19 and 5.20. A similar result for the cutoff frequency is shown in Figure 5.21 with the UFET model predicting the trends well.

5.3 Operational Amplifier Sensitivity Study

In order to demonstrate the utility of UFET in a circuit application, an operational amplifier [All87] is examined to determine the variation in circuit performance in relation to process variations. The CMOS operational amplifier

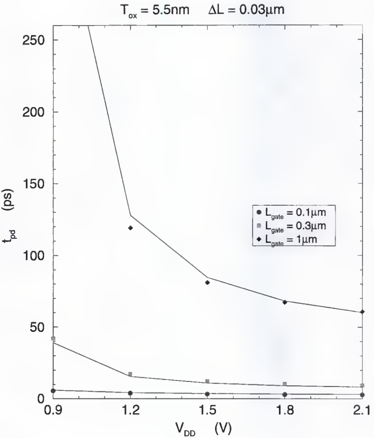

Figure 5.16 UFET-(lines) and MEDICI-(points)simulated intrinsic pull-down delay in 0.1μm technology with t_{ox} = 5.5nm.

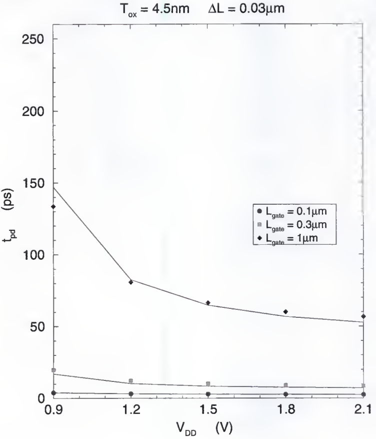

Figure 5.17 UFET-(lines) and MEDICI-(points)simulated intrinsic pull-down delay in 0.1μm technology with t_{ox} = 4.5nm.

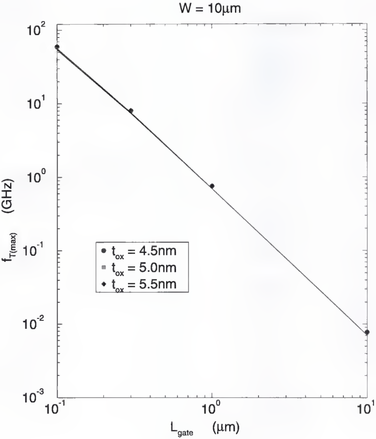

Figure 5.18 UFET-(lines) and MEDICI-(points)simulated cutoff frequency in 0.1μm technology with 10% oxide thickness variations.

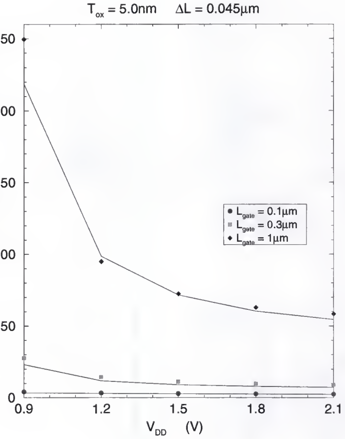

Figure 5.19 UFET-(lines) and MEDICI-(points)simulated intrinsic pull-down delay in 0.1μm technology with ΔL = 0.045μm.

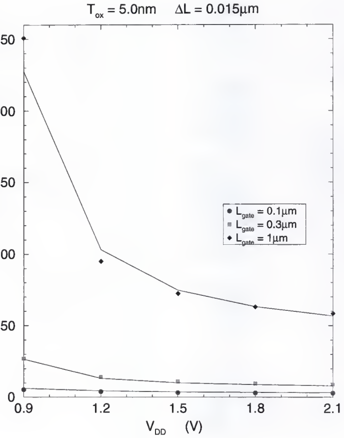

Figure 5.20 UFET-(lines) and MEDICI-(points)simulated intrinsic pull-down delay in 0.1μm technology with ΔL = 0.015μm.

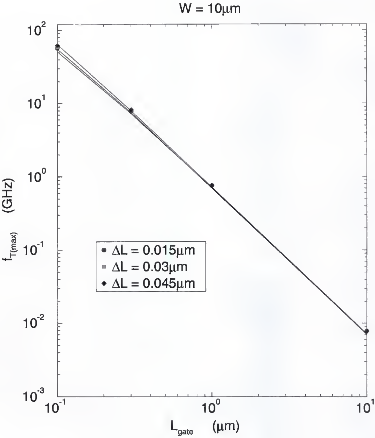

Figure 5.21 UFET-(lines) and MEDICI-(points)simulated cutoff frequency in 0.1μm technology with ΔL 50% variations.

designed using normalized channel lengths and presented at a SEMATECH workshop (B. M. Tenbroek, private communication, 1997) is chosen; the schematic is shown in Figure 5.22. Since UFET is process-based, the sensitivity study is a relatively straightforward process since the model parameters are strongly correlated with the process variables.

The operational amplifier is a two-stage folded cascode design. The first (input) stage consists of a differential PMOS pair with an active load. The cascode circuit increases the gain of the first stage by increasing the output resistance seen by the first stage. The second stage (output) stage is a simple class-A amplifier. The compensation is provided by the capacitor in series with a PMOS transistor which cancels the non-dominant pole to improve the phase margin of the circuit [All87]. In addition, there are several NMOS transistors which function as the bias circuit for the operational amplifier.

5.3.1 Process Variations

Using the 0.15μm technology presented in Chapter 4, a subset of the process variables (t_{ox}, ΔL_{NMOS}, ΔL_{PMOS}, $N_{POLY,NMOS}$ and $N_{POLY,PMOS}$) is selected. Of these, the largest uncontrolled process variation is the lateral diffusion which affects the threshold voltage in extremely scaled devices and the overlap capacitances which become more important in extremely scaled devices. Variations in oxide thickness and polysilicon-gate doping concentration also lead to variations in threshold voltage.

Although only NMOS devices were calibrated, the PMOS devices are assumed to be "symmetric" with a 60% reduction in the mobility, i.e., all model

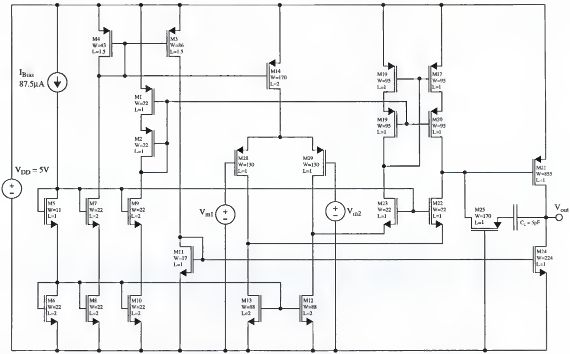

Figure 5.22 2-Stage Folded Cascode Operational Amplifier with normalized channel length; L=0.15µm is used for the simulations.

parameters are the same except for a mobility reduction. In addition, the contact resistance problem seen in the data is ignored, and the same model parameters are used for all channel lengths. Based on published process variations [Rio95, Aro95], variations in the process variables of interest are set. The oxide thickness is presumed to vary by 10% from the nominal process value of 2.7nm, and the lateral diffusion lengths for both devices are assumed to vary by 50% from the nominal value of 0.03μm. The influence of the polysilicon-gate depletion effect on the circuit performance is examined by varying the polysilicon-gate doping concentrations from $1\times10^{19}\text{cm}^{-3}$ (severe gate depletion effects) to $1\times10^{20}\text{cm}^{-3}$ (negligible gate depletion effects).

5.3.2 Sensitivity Results

Using the presumed process variations, three figures of merit important to analog circuit designers (DC gain, unity gain frequency and phase margin) are examined to determine their dependencies on process variations. The results could then be used by a circuit designer to determine if the operational amplifier needs to be redesigned in order to better tolerate the process variations.

Using the nominal technology channel (L = 0.15μm) with the nominal process values results in an operational amplifier with a good DC gain (75dB), unity gain frequency (42MHz) and phase margin (90°) as shown by the UFET simulation results in Figures 5.23 and 5.24. Although these results indicate that the operational amplifier may be over-compensated as implied by the large phase margin, the pole-zero cancellation circuit is not optimally designed since the channel resistance is

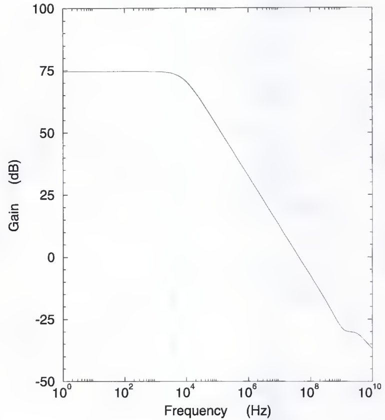

Figure 5.23 UFET-simulated open loop gain for nominal 0.15μm technology.

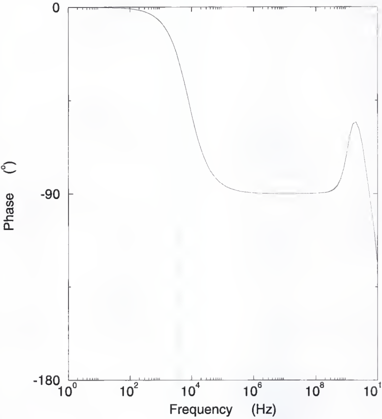

Figure 5.24 UFET-simulated open loop phase for nominal 0.15μm technology.

smaller than anticipated due to the effects of ΔL. Examination of the correlation between phase margin and the process variations may indicate a reduction in the value of the compensation capacitor is possible which will reduce the circuit area and increase the slew rate [All87] after the circuit has been redesigned.

Over the process variations in the gate oxide thickness, the DC gain shows a small sensitivity as illustrated in Figure 5.25 with a larger sensitivity for the unity gain frequency. Since the main purpose of the NMOS transistors is to control the bias conditions (as forced by I_{Bias} in Figure 5.22), there is little sensitivity to the process variations associated with the NMOS devices. This is shown for variations of NMOS lateral diffusion in Figure 5.26 and for N_{POLY} in Figure 5.27. The PMOS transistors control the dominant portions of the operational amplifier circuit, and it is expected that there will be a larger sensitivity for these devices than for the NMOS. This is true for both the PMOS lateral diffusion and PMOS polysilicon-gate doping as shown in Figures 5.28 and 5.29.

Using the results of this sensitivity study allows a series of recommendations to be made regarding design improvements for this circuit. The circuit is relatively insensitive to t_{ox} and ΔL_{NMOS} variations in the process. It is also relatively insensitive to $N_{POLY,NMOS}$ and $N_{POLY,PMOS}$ for doping concentrations larger than $3\times10^{19}\text{cm}^{-3}$, which are easily achieved [Aro95]. However, the design is sensitive to variations in the PMOS lateral diffusion, and the circuit should be redesigned to reduce this sensitivity. This is accomplished by increasing the channel lengths and widths of the PMOS devices controlling the circuit performance. This will decrease the sensitivity of the circuit at the penalty of increased area. However,

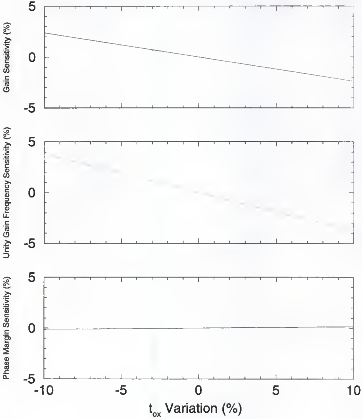

Figure 5.25 UFET-simulated t_{ox} sensitivity.

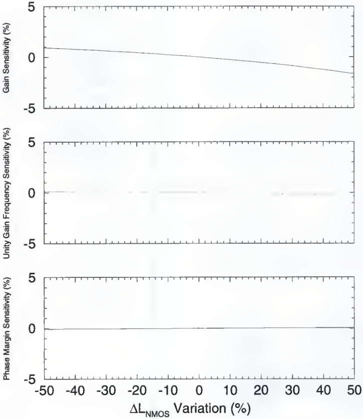

Figure 5.26 UFET-simulated ΔL_{NMOS} sensitivity.

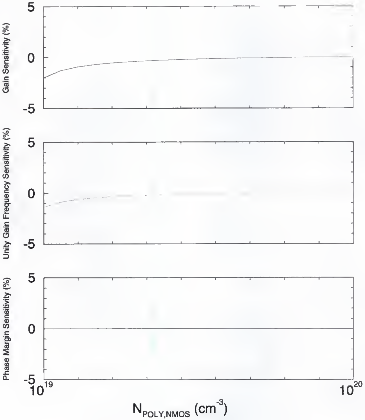

Figure 5.27 UFET-simulated $N_{POLY,NMOS}$ sensitivity.

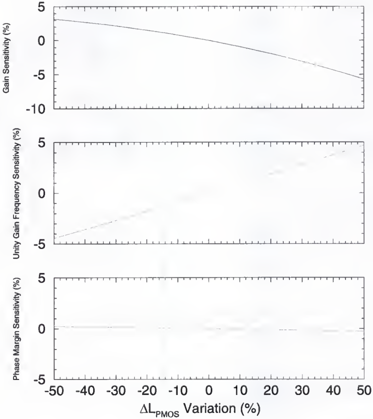

Figure 5.28 UFET-simulated ΔL_{PMOS} sensitivity.

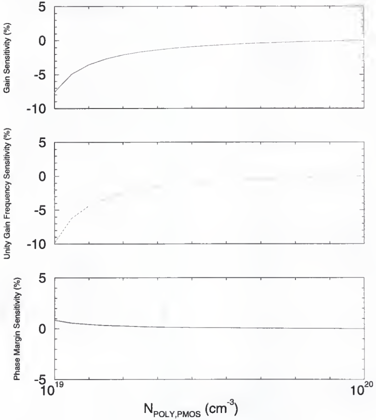

Figure 5.29 UFET-simulated $N_{POLY,PMOS}$ sensitivity.

the results also show that the circuit is over-compensated, and the increased area can be partially offset by reducing the size of the compensation capacitor. The resulting operational amplifier using 0.45μm for the normalized channel lengths in the PMOS devices has improved DC gain (86dB), a smaller unity gain frequency (37MHz) and a similar phase margin (87^o), but more importantly the circuit sensitivity to ΔL_{PMOS} has been greatly reduced as shown in Figure 5.30. The problem with the pole-zero cancellation has also been eliminated as shown in the gain and phase plots Figures 5.31 and 5.32.

5.4 Conclusion

UFET's small number of process-based parameters simplify the parameter extraction/evaluation procedure, and the correlation to process parameters enable UFET to be easily used in modeling device sensitivity. This was demonstrated with a MEDICI exercise where UFET was used to simulate an extremely scaled technology, and to also examine device sensitivity to variations in the oxide thickness and lateral diffusion in this technology. This demonstration was then extended by using UFET to examine the sensitivity of a CMOS operational amplifier to normal process variations. The results show that UFET can be a viable alternative to the continued use of empirical compact models for both circuit simulation and device sensitivity studies.

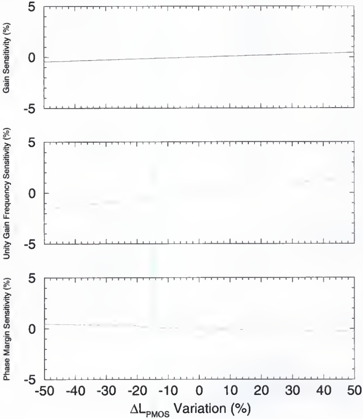

Figure 5.30 UFET-simulated ΔL_{PMOS} sensitivity in the redesigned circuit.

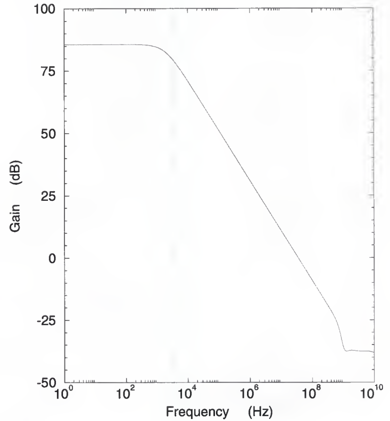

Figure 5.31 UFET-simulated open loop gain for redesigned 0.15µm technology.

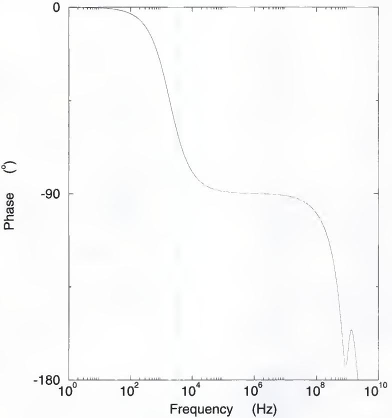

Figure 5.32 UFET-simulated open loop phase for redesigned 0.15μm technology.

CHAPTER 6
CONCLUSIONS AND RECOMMENDATIONS FOR FUTURE WORK

6.1 Conclusions

The many deficiencies of existing compact short-channel MOSFET models imply the need for a new physical, predictive model. This dissertation presented such a model for deep-submicron devices (UFET) with C_∞ continuity that relies on approximate two-dimensional analyses, which are computationally efficient, to account for the predominant short-channel effects. These solutions of two-dimensional analyses are physically linked and are expressed in simple terms that yield physical insight into device behavior as well as a predictive circuit model with utility for TCAD, e.g., for statistical simulations and circuit sensitivity analyses, as well as design. The parameter-evaluation procedure was outlined, and the advantages of a physical model where the process-based model parameters are closely tied to the device physics and structure were demonstrated. This is in contrast to models such as BSIM3 [Che96] which are dependent on extensive parameter optimization that can lead to non-physical parameter sets. Validation of UFET was then presented using device simulations and measured data, and the utility of the model was shown through a MEDICI benchmark and a sensitivity analysis of a CMOS operational amplifier. The UFET model implemented in the Type-I interface is available from the UF SOI Group at the University of Florida.

6.2 Recommendations for Future Work

Although much progress was made in the development of the UFET MOSFET model, there is still much more work to be done in order to make it the model of choice for modeling deep-submicron MOSFETs. The focus of this work was the development of a process-based MOSFET model with C_∞ continuity. The next phase of this research should focus on the effects which were not included or not well modeled in UFET. Along with upgrading the extrinsic portions of the model, this will make UFET a complete MOSFET model for deep-submicron technologies which can be accepted as the industry standard.

The areas for further UFET investigation are listed below in order of importance

- RSCE/halo effects
- Overlap and fringing capacitances
- Narrow width effects
- Non-local effects: velocity overshoot and impact ionization
- Explicit accounting for depletion charge variation along channel
- Leakage current and junction perimeters
- Tunneling currents
- Noise modeling

The big hurdle for physical MOSFET modeling is the Reverse Short-Channel Effect due to Transient Enhanced Diffusion and the introduction of nonuniform lateral doping profiles, i.e., halos, which result in a changing device structure as a function of channel length. Although a preliminary model for this effect was implemented in the UFET formalism, the comparisons with measured data suggest that the RSCE model should be improved.

At this time, all of the effects in UFET are based on local-field models. The non-local impact-ionization model in UFSOI [Fos97] should be made consistent with the UFET modeling approach in order to account for the non-local effects in extremely scaled devices.

It will also be necessary to improve the modeling of the extrinsic portions of the device. The overlap capacitances are modeled as simple parallel-plate capacitors, and the fringing capacitances are ignored. The overlap capacitances are bias-dependent and should be modeled as such. Due to significant errors in the reverse-bias junction leakage current, an approach similar to that in the UFSOI models should be implemented where physical models for generation and recombination are used. This upgrade should also account for the perimeter components in the leakage current and the junction depletion charges. It is also necessary to account for the narrow-width effects that are seen in measured devices due to the three-dimensional effects associated with the isolation structures. The tunneling currents associated with the scaled gate oxides should be accounted for, and the GIDL model currently being implemented in UFSOI should be added to UFET when the development is complete.

The channel-current analysis can also be upgraded through the explicit integration of the depletion charge along the channel rather than assuming a constant depletion capacitance. Although this will (slightly) complicate the analysis for $\Delta\psi_s^{sat}$, the trade-off for increased accuracy seems reasonable.

At present, UFET lacks a noise model. The thermal noise should be modeled as proposed by Tsividis [Tsi87]:

$$\Delta i^2 = \frac{4kT\mu|Q_i|}{L^2}\Delta f. \tag{6.1}$$

It is also recommended that the implementation of non-quasi-static effects be examined in order to confidently use the models for high-frequency analog design.

Although the UFET model has been moved from MMSPICE into the API, where the model is not completely isolated from the simulator, this process needs to be continued with UFET moving along to the next interface standard (either Type-II, Verilog, MAST or some similar approach), which will allow the model to be designed without regard to the simulation platform used. It is also a necessity that the parameter-evaluation procedure outlined in Chapter 4 be implemented in software (e.g., UTMOST, or a similar package). This will enable UFET to be more easily distributed and used effectively and pervasively in industry.

REFERENCES

[All87] Phillip E. Allen and Douglas R. Holberg, CMOS Analog Circuit Design, Fort Worth, Texas, Harcourt Brace Jovanovich College Publishers, 1987.

[Aro87] N. Arora, "Semi-Empirical Model for the Threshold Voltage of a Double Implanted MOSFET and Its Temperature Dependence," Solid-State Electronics, Vol. 30, No. 5, p. 559, 1987.

[Aro94] N. Arora, R. Rios, C. Huang and K. Raol, "PCIM: A Physically Based Continuous Short-Channel IGFET Model for Circuit Simulation," IEEE Transactions on Electron Devices, Vol. 41, No. 6, p. 988, June 1994.

[Aro95] N. Arora, R. Rios and C. Huang, "Modeling the Polysilicon Depletion Effect and Its Impact on Submicrometer CMOS Circuit Performance," IEEE Transactions on Electron Devices, Vol. 42, No. 5, p. 935, May 1995.

[Bre78] J. Brews, "A Charge-Sheet Model of the MOSFET," Solid-State Electronics, Vol. 21, p. 927, 1978.

[Bru95] H. Brut, A, Juge and G. Ghibaudo, "Physical Model of Threshold Voltage in Silicon MOS Transistors Including Reverse Short Channel Effect," Electronics Letters, Vol. 31, No. 5, p. 411, 1995.

[Bur89] Richard L. Burden and J. Douglas Faires, Numerical Analysis, Boston, PWS-K, 1989.

[Cha97] Duckhyun Chang, "Pragmatic and Reliable Device/Circuit Simulation for Design in Advanced Silicon-Based Technologies," Ph.D. Dissertation, University of Florida, Gainesville, 1997.

[Che96] Yuhua Cheng, Mansun Chan, Kelvin Hui, Min-Chie Jeng, Zhihong Liu, Jianhui Huang, Kai Chen, James Chen, Robert Tu, Ping K. Ko, and Chenming Hu, "BSIM3v3 Manual," University of California, Berkeley, 1996.

[Cho91] J. Y. Choi, Modeling and Simulation of the Fully Depleted Silicon-on-Insulator MOSFET for Submicron CMOS IC Design," Ph.D. Dissertation, University of Florida, Gainesville, 1991.

[Cod85] C. Codella and S. Ogura, "Halo Doping Effects in Submicron DI-LDD Device Design," IEDM Technical Digest, p. 230, Washington, D.C., 1985.

[Dor94] M. van Dort, P. Woerlee and A. Walker, "A Simple Model for Quantization Effects in Heavily-Doped Silicon MOSFETs at Inversion Conditions," Solid-State Electronics, Vol. 37, No. 3, p. 411, March 1994.

[ElM77] Y. A. El-Mansy and A. R. Boothroyd, "A Simple Two-Dimensional Model for IGFET Operation in the Saturation Region," IEEE Transactions on Electron Devices, Vol. ED-24, p. 254, 1977.

[Fos94] Jerry G. Fossum, G.-B. Hong and Keith R. Green, "MMSPICE-3.0: User's Guide," University of Florida, Gainesville, 1994.

[Fos97] Jerry G. Fossum, Duckhyun Chang, Srinath Krishnan, Dongwook Suh, Glen Workman and Ping-Chen Yeh, "SOISPICE-4.4: User's Guide," University of Florida, Gainesville, 1997.

[Get78] I. E. Getreu, Modeling the Bipolar Transistor, New York, Elsevier, 1978.

[Gra93] Paul R. Gray and Robert G. Meyer, Analysis and Design of Analog Integrated Circuits, Third Edition, New York, John Wiley and Sons, Inc., 1993.

[Gre90] K. R. Green, "SUMM: A SUPREM-3/MMSPICE-I Integrator for Bipolar Technology CAD," M.S. Thesis, University of Florida, Gainesville, 1990.

[Gre93a] Keith R. Green, "A Model of the Short-Channel, Metal-Oxide-Semiconductor Field-Effect Transistor for Pragmatic Mixed-Mode Device/Circuit Simulation," Ph.D. Dissertation, University of Florida, Gainesville, 1993.

[Gre93b] Keith R. Green and Jerry G. Fossum, "A Simple Two-Dimensional Model for Subthreshold Channel-Length Modulation in Short-Channel MOSFET's," IEEE Transactions on Electron Devices, Vol. 40, No. 8, August 1993, pp. 1561-1563.

[Haj79] I. N. Hajj and S. Skelboe, "Time-domain analysis of nonlinear systems with finite number of continuous derivatives," IEEE Transactions on Circuits and Systems, Vol. CAS-26, pp. 297-303, 1979.

[Hon94] G.-B. Hong, "Modeling, Simulation and Design of SiGe-based Hetero-Junction Bipolar Transistors for High-Performance Integrated Circuits," Ph.D. Dissertation, University of Florida, Gainesville, 1994.

[Hua93] C. Huang and N. Arora, "Measurements and Modeling of MOSFET I-V Characteristics with Polysilicon Depletion Effect," IEEE Transactions on Electron Devices, Vol. 40, No. 12, p. 2330, December 1993.

[Iwa93] Masao Iwase, Tomohisa Mizuno, Minoru Takhashi, Hiromi Niiyama, Masato Fukumoto, Katsuhiro Ishida, Satoshi Inaba, Yuji Takigami, Atsuo Sanda, Akira Toriumi and Makoto Yoshimi, "High-Performance

0.10μm CMOS Devices Operating at Room Temperature," IEEE Electron Device Letters, Vol. 14, No. 2, p. 51, 1993.

[Jan97] Sheng-Lyang Jang and Man-Chun Hu, "An Analytical Drain Current Model for Submicrometer and Deep Submicrometer MOSFET's," IEEE Transactions on Electron Devices, Vol. 44, No. 11, p. 1896, November, 1997.

[Jeo89] H. Jeong, "MMSPICE: A Physical Alternative to Gummel-Poon/ SPICE and a Semi-Numerical Mixed-Mode Simulator for Advanced Bipolar Technology CAD," Ph.D. Dissertation, University of Florida, Gainesville, 1989.

[Kha93] Manoj K. Khana, S. Haldar, Maneesha, Rachna Sood and R. S. Gupta, "Substrate-Bias-Dependent Threshold-Voltage Model of Short-Channel MOSFET," Solid-State Electronics, Vol. 36, No. 4, pp. 661-664, 1993.

[Liu93] Zhi-Hong Liu, Chenming Hu, Jian-Hui Huang, Tung-Yi Chan, Min-Chie Jeng, Ping K. Ko and Y. C. Cheng., "Threshold Voltage Model for Deep-Submicrometer MOSFETs," IEEE Transactions on Electron Devices, Vol. 40, No. 1, January 1993, pp. 86-94.

[Lun96] M. Lundstrom, "Scattering Theory of Short-Channel MOSFETs," IEDM Technical Digest, p.387, San Francisco, 1996.

[Mar88] J. Mar, "CAD for Manufacturing: Why Its Time Is Now," TECHCON Abstracts, p. 277, Dallas, 1988.

[McA91] C. McAndrew, B. Bhattacharyya and O. Wing, "A Single-Piece C_∞-Continuous MOSFET Model Including Subthreshold Conduction," IEEE Electron Devices Letters, Vol. 12, No. 10, p. 565, October 1991.

[McA93] C. McAndrew, B. Bhattacharyya and O. Wing, "A C_∞-Continuous Depletion Capacitance Model," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 12, No. 6, June 1993.

[Mii94] Y. Mii, S. Rishton, Y. Taur, D. Kern, T. Lii, K. Lee, K. A. Jenkins, D. Quinlan, T. Brown Jr., D. Danner, F. Sewell and M. Polcari, "Experimental High Performance Sub-0.1mm Channel nMOSFETs," IEEE Electron Device Letters, Vol. 15, No. 1, p. 28, 1994.

[Nag75] L. W. Nagel, "SPICE2: A Computer Program to Simulate Semiconductor Circuits," Research Lab Memo ERL-M520, University of California, Berkeley, 1975.

[New95] David Newmark, "Simulator Independent MOSFET Model Type-1 Standard," Motorola APRDL/CMG Report, Austin, TX, 1995.

[Niu97] G. F. Niu, R. M. M. Chen, G. Ruan and T. A. Tang, "Definition of Effective Channel Length (L_{eff}) in Deep Submicron MOSFETs Based on Numerically Simulated Surface Potential," Solid-State Electronics, Vol. 41, No. 9, pp. 1377-1382, 1997.

[Oh80] S.-Y. Oh, D. E. Ward and R. W. Dutton, "Transient Analysis of MOS Transistors," IEEE Transactions on Electron Devices, Vol. 27, pp. 1571-1578, 1980.

[Ong87] Tong-Chern Ong, Ping K. Ko and Chenming Hu, "50Å Gate-Oxide MOSFET's at 77K," IEEE Transactions on Electron Devices, Vol. 34, No. 10, pp. 2129-2135, October 1987.

[Orl87] M. Orlowski, C. Mazure and F. Lau, "Submicron Short-Channel Effects Due to Gate Reoxidation Induced Lateral Interstitial Diffusion," IEDM Technical Digest, p. 632, Washington, D.C., 1987.

[Pao66] H. C. Pao and C. T. Sah, "Effects of Diffusion Current on Characteristics of Metal-Oxide (Insulator)-Semiconductor Transistors," Solid-State Electronics, Vol. 9, p. 927, 1966.

[Qua92] T. Quarles, A. R. Newton, D. O. Pederson and A. Sangiovanni-Vincentelli, "SPICE3 User's Manual," University of California, Berkeley, 1992.

[Rat82] K. N. Ratnakumar and James D. Meindl, "Short-Channel MOST Threshold Voltage Model," IEEE Journal of Solid State Circuits, Vol. 17, No. 5, October 1982, pp. 937-948.

[Rei96] Guenter Reichert and Thierry Ouisse, "Relationship Between Empirical and Theoretical Mobility Models in Silicon Inversion Layers," IEEE Transactions on Electron Devices, Vol. 43, No. 9, September 1996, pp. 1394-1398.

[Rio95] R. Rios, N. Arora, C. Huang, N. Khalil, J. Faracelli and L. Gruber, "A Physical Compact MOSFET Model, Including Quantum Mechanical Effects, for Statistical Circuit Design Applications," IEDM Technical Digest, p. 937, Washington, D.C., 1995.

[Sch93] K. Schuegraf, C. King and C. Hu, "Impact of Polysilicon Depletion in Thin Oxide MOS Technology," Proceedings of the 1993 International Symposium on VLSI Technology, Systems and Applications, Taiwan, p. 86, 1993.

[Sha96] Prashant Shamarao and Mehmet C. Öztürk, "A Study on Channel Design for 0.1µm Buried p-Channel MOSFET's," IEEE Transactions on Electron Devices, Vol. ED-43, p. 1942, 1996.

[Sze81] S. M. Sze, Physics of Semiconductor Devices, Second Edition, New York, Wiley, 1981.

[Taur97] Yuan Tar and Edward Nowak, "CMOS Devices below 0.1µm: How High Will Performance Go?," IEDM Technical Digest, p. 215, Washington, D.C., 1997.

[Tay78] G. W. Taylor, "Subthreshold Conduction in MOSFET's," IEEE Transactions on Electron Devices, Vol. ED-25, p. 337, 1978.

[Tec89] Technology Modeling Associates, Inc., "TMA Supreme," Palo Alto, CA, 1989.

[Tec92] Technology Modeling Associates, Inc., "TMA MEDICI Two-Dimensional Device Simulation Program," Palo Alto, CA, 1992.

[Tro79] R. R. Troutman, "VLSI Limitations from Drain-Induced Barrier Lowering," IEEE Transactions on Electron Devices, Vol. ED-26, p. 461, 1979.

[Tsi82] Yannis Tsividis, "Moderate Inversion in MOS Devices," Solid-State Electronics, Vol. 25, No. 11, November 1982, pp. 1099-1104.

[Tsi87] Yannis Tsividis, Operation and Modeling of the MOS Transistor, New York, McGraw-Hill 1987.

[Tsi94] Yannis Tsividis and Ken Suyama, "MOSFET Modeling for Analog Circuit CAD: Problems and Prospects," IEEE Journal of Solid-State Circuits, Vol. 29, No. 3, March 1994, pp. 210-216.

[Vee88] Surya Veeraraghavan and Jerry G. Fossum, "A Physical Short-Channel Model for the Thin-Film SOI MOSFET Applicable to Device and Circuit CAD," IEEE Transactions on Electron Devices, Vol. 35, No. 11, November 1988, pp.1866-1875.

[Ven95] S. Venkatesan, J. W. Lutze, C. Lage and W. J. Taylor, "Device Drive Current Degradation Observed with Retrograde Channel Profiles," IEDM Technical Digest, p. 419, Washington, D.C., 1995.

[Vis85] C. R. Viswanathan, Bruce C. Burkey, Gerrit Lubberts and Timothy J. Tredwell, "Threshold Voltage in Short-channel MOS Devices," IEEE Transactions on Electron Devices, Vol. 32, No. 5, May 1985, pp. 932-940.

[Wor98] G. O. Workman, J. G. Fossum, S. Krishnan, and M. M. Pelella, "Physical Modeling of Temperature Dependences of SOI CMOS Devices and Circuits Including Self-Heating,", IEEE Transactions on Electron Devices, to be published January, 1998.

[Yan91] R. Yan, A. Ourmazd and D. Jeon, "Scaling the Si metal-oxide-semiconductor field-effect-transistor into the 0.1-μm regime using vertical doping engineering," Applied Physics Letters, pp. 3315-3317, Dec. 1991.

[Yan92] R. Yan, A. Ourmazd and K. Lee, "Scaling the SI MOSFET: From Bulk to SOI to Bulk," IEEE Transactions on Electron Devices, Vol. 39, pp. 1704-1710, July 1992.

[Yau74] L. D. Yau, "A Simple Theory to Predict the Threshold Voltage of Short-Channel IGFET's," Solid-State Electronics, Vol. 17, 1974, pp. 1059-1063.

BIOGRAPHICAL SKETCH

Douglas Aaron Weiser was born in Winchester, Indiana, on October 23, 1968. He received the B.S. degree in electrical engineering from Rose-Hulman Institute of Technology, Terre Haute, Indiana, in 1990. Before returning to graduate school he was with Westinghouse, Baltimore, Maryland, where he was involved with building and testing a Navy sonar system. From August 1991 to August 1993, he was working toward the M.S. degree at the University of Florida, Gainesville, in the area of efficient simulation of distributed power semiconductor devices. Since 1993, he has been working toward the Ph.D. degree at the University of Florida, Gainesville. In 1996, he was awarded the Ross Fellowship which allowed him to extend the collaboration between the University of Florida and Leti, Grenoble, France, where he was a visiting researcher involved with SOI technologies for seven months. After graduation, he will be employed at Texas Instruments, Dallas, working on RF MOSFET modeling.

He is a member of IEEE, Tau Beta Pi and Eta Kappa Nu.

I certify that I have read this study and that in my opinion it conforms to acceptable standards of scholarly presentation and is fully adequate, in scope and quality, as a dissertation for the degree of Doctor of Philosophy.

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